Towards Dark Silicon Era in FPGAs Using Complementary Hard Logic Design

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***Abstract*—While the transistor density continues to grow exponentially in *Field-Programmable Gate Arrays* (FPGAs), the increased leakage current of CMOS transistors act as a *power wall* for the aggressive integration of transistors in a single die. One recently trend to alleviate the power wall in FPGAs is to turn off inactive regions of the silicon die, referred to as *dark silicon*. This paper presents a reconfigurable architecture to enable effective fine-grained power gating of unused *Logic Blocks* (LBs) in FPGAs. In the proposed architecture, the traditional soft logic is replaced with *Mega Cells* (MCs), each consists of a set of complementary *Generic Reconfigurable Hard Logic* (GRHL) and a conventional *Look-Up Table* (LUT). Both GRHL cells and LUTs can be power gated and turned off by controlling configuration bits. In the proposed MC, only one cell is active and the others are turned off. Experimental results on MCNC benchmark suite reveal that the proposed architecture reduces the critical path delay, power, and *Power Delay Product* (PDP) of LBs up to 5.3%, 30.4%, and 28.8% as compared to the equivalent LUT-based architecture.**

I. Introduction

In the past decade, power consumption has turned to be one of the primary design constraints of *Field-Programmable Gate Arrays* (FPGAs), as *Dennard* scaling ceases to hold in the recent technology nodes [1]. Due to almost constant power budget of *Integrated Circuits* (ICs) in different application domains [2], the leakage current of *Complementary Metal-Oxide Semiconductor* (CMOS) transistors will act as a *power wall* for further integration of transistors in a single die. Hence, the exponential growth of transistor density will be slowed down unless a significant portion of the silicon die is powered off. This phenomena which is also referred to as *dark silicon* [2] can significantly limit the proportionate increase in the performance and the functionality of the ICs [2]. In particular, the state-of-the-art FPGAs have the industry record of the number of transistors in a single chip [3] and as such, their high power demand will be a severe challenge in the dark silicon era.

A logic function in conventional FPGAs is typically implemented by configuring an N-input LUT (LUT-N). A LUT-N which consists of 2^N configuration bits, can implement any arbitrary N input logic function. Such flexibility in logic mapping comes with up to two orders of magnitude in power and area overheads as compared to *Application-Specific Integrated Circuit* (ASIC) implementation [4]. In addition, no fine- or coarse-grained power gating is currently implemented in the state-of-the art FPGAs. Therefore, all resources, regardless of being utilized or not, consume static power, which makes the static power the dominant power factor in FPGAs [5].

Previous studies on alternative structures for soft logic in FPGAs were primarily focused on improving the performance and the area efficiency of soft logic in FPGAs. These solutions can be classified into four major categories: *Application Specific Hard Logic* (ASHL) [6], [7], shadow clusters [8], [9], *Extended-LUTs* (E-LUTs) [10], [11], and *Generic Reconfigurable Hard Logic* (GRHL) [12]–[14]. These structures are targeted to mainly improve performance and area overheads of the FPGAs and hence, can even impose power overheads. In addition, the static power of unused resources is not considered in these solutions. Another class of techniques tries to reduce the static power consumption of FPGAs by power gating the unused resources [5], [15], [16]. Nonetheless, the power and performance efficiency of used resources is not addressed in such techniques.

This paper presents a reconfigurable architecture to explicitly address the power efficiency of FPGAs to enable fine-grained power gating of both unused (complete) and used (partial) *Logic Blocks* (LBs) in FPGAs. In this architecture, a *Mega Cell* (MC) is proposed as a replacement for the conventional LUTs. The proposed MC consists of two GRHLs, one LUT, and a configurable control unit. In the proposed architecture, the logic functions are mapped to either one of the GRHLs or the LUT cell. The GRHL cells are designed such that more than 94% of logic functions are mapped to them and only less than 6% of the functions are mapped to the LUT cells of the MCs. The controller is designed such that at most one cell is active and the other cells are power gated. The MCs that are not utilized in a design, are completely powered off through their controllers. The proposed architecture not only improves the power efficiency of unused MC, but also improves both power and performance efficiency of used MCs as compared to the conventional LUT-based architecture. The experimental results based on detailed SPICE-level analysis show that the proposed architecture improves the performance, power, and *Power Delay Product* (PDP) of LBs up to 35.8%, 65.6%, and 78.4%, respectively, as compared to the LUT-6 based architecture.

The rest of this paper is organized as follow. In Sec. II, the proposed MC and the methodology of designing GRHLs are discussed. Sec. III presents the implementation of the proposed MC for a set of benchmark applications and its experimental results. Sec. IV discusses the limitations of the current work. Finally, Sec. V concludes the paper and presents the future work.

II. Proposed Architecture

The main purpose of the proposed architecture is to reduce the overall power consumption of LBs in the FPGAs by replacing each LUT with an MC. The proposed MC consists of a set of GRHLs, a LUT cell, and *Power-Controlling Configuration Bits* (PCCBs). Each PCCB controls the power supply of either

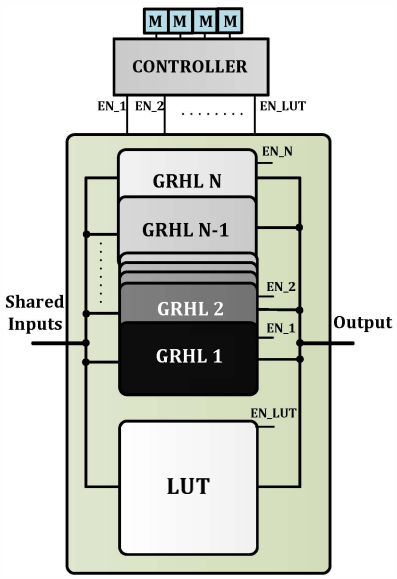


Fig. 1. Overall structure of an MC

a GRHL or the LUT cell in the MC. PCCBs are configured at the reconfiguration time to activate or deactivate (power gate) the corresponding GRHL or LUT cell in the MC. In the proposed architecture, the unused GRHL and LUT cells are power gated to reduce the static power consumption. In addition, by appropriately configuring the controlling bits, one can ensure that at most one GRHL or LUT cell will be active at a time in the MC. As a result, the proposed architecture not only reduces the power consumption of unused MCs but also reduces the power consumption of used MCs as compared to the traditional LUT-based architecture.

In the subsequent subsections, we will discuss the design methodology of the MCs and the design constrains.

A. MC Design Methodology

In the proposed architecture, each LUT cell is replaced with an MC. The MC includes a set of GRHLs and one LUT cell. Both GRHLs and the LUT cell share the same inputs. Each GRHL should implement a portion of a LUT functionality with less power overheads as compared to a LUT cell. Fig. 1 illustrates the overall structure of an MC. GRHLs have less flexibility as compared to the soft logic but they can instead implement the functions more power efficiently than LUTs. There is a trade-off between power efficiency of GRHLs and their flexibility (logic mapping capability).

By reducing the flexibility of GRHLs, a specific subset of functions is implemented more power-efficiently. This, however, reduces the utilization probability of GRHLs. Moreover, one can use various GRHLs in the MC to increase the utilization probability of the GRHLs. Increasing the number of GRHLs comes with the cost of more sophisticated controller. This can adversely affect the overall power consumption improvements in the MC. Note that by exploiting LUT along with GRHLs in the MC, if a function cannot be mapped to any of GRHLs, it will be mapped to the LUT. Therefore, the flexibility is not compromised.

Equation 1 and Equation 2 demonstrate the design constrains of an MC. In these equations, $Cell_i$ could be either one of the GRHLs or the LUT cell in the MC. Assuming N is the number of cells in the MC, $Power_{Cell_i}$ is the power consumption of $Cell_i$ in its active mode and P_{Cell_i} is the utilization probability of $Cell_i$.

$$\sum_{i=1}^{i=N} Power_{Cell_i} \times P_{Cell_i} + Power_{Controller} \ll Power_{LUT} \tag{1}$$

$$\sum_{i=1}^{i=N} P_{Cell_i} = 1 \tag{2}$$

The utilization probability of each GRHL highly depends on the coverage ratio of the target GRHLs. The coverage ratio is defined as the ratio of the functions which can be implemented by a GRHL to the total number of functions exist in the target circuits. Since GRHLs cannot cover all possible functions, to provide the required flexibility, one would need to include a LUT in the MC. However, the mapper should try to map the function to GRHLs first and if not possible, use the LUT. This way the power consumption can be reduced while the flexibility is not affected. Implementing this scheme in the mapper will reduce P_{LUT} and consequently will increase P_{GRHLs}. To achieve high P_{GRHLs}, GRHLs should be designed in a way which leads to the maximum coverage ratio. The maximum coverage ratio should be achieved while keeping power consumption overheads minimal.

B. Design of GRHLs

The first step in designing GRHLs is classifying functions which could be implemented by a single GRHL cell. In this work, same as [12], [14], we classify logic functions based on *Negation-Permutation-Negation* (NPN) classes. By definition, two functions A and B belong to the same NPN class if A could be derived by *Negating* inputs, *Permuting* inputs, and/or *Negating* the output of B and vice versa. For instance, $ABC + D$ and $(A + D + C)B$ belong to the same NPN class and are NPN equivalent. The main advantage of using NPN classes for designing GRHLs in reconfigurable architectures is that permuting inputs could be provided by the reconfigurable routing resources of reconfigurable architectures. Moreover, the negation of inputs and outputs could be implemented by the means of configurable inverters.

In the state-of-the art FPGAs, LUT-6 cells are widely used because LUT-6 provides the best performance among LUT-K cells [17]. Nonetheless, LUT-4 cells are the best choice if the area efficiency is targeted [17]. There exists 34,225 NPN classes for 6-input functions and at least 311 NPN classes should be supported by GRHLs to reach 90% coverage ratio [18]. Note that adding more GRHLs to reach higher coverage ratio results in more area overheard, and more complicated controller, which in turn affects the power efficiency. As a result, finding a subset of 6-input GRHLs which can cover a considerable portion of 6-input functions will not be advantageous.

Unlike 6-input functions, 65,536 ($= 2^{16}$) 4-input functions could be classified under only 222 NPN classes [18]. In addition, as it will be shown next, more than 90% of 4-input functions could be implemented by only two 4-input GRHLs. GRHLs have typically less propagation delay as compared

to LUT-4 cells. Consequently, the overall performance of the MC-based architecture could be comparable with LUT-6 based architectures which conventionally offer best performance efficiency. Hence, we will focus on 4-input GRHLs and NPN classes.

C. Proposed Controller

Fig. 2 illustrates the overall structure of an LB consists of a cluster of MCs. Each PCCB corresponds to one cell in the MC. The value of the PCCB indicates whether the GRHL or LUT cell should be disabled or not. In the proposed MC, the logical values of 0 and 1 are opted to represent OFF (disable) and ON (enable) states of PCCBs, respectively. The configuration of PCCBs is determined at the configuration time of FPGA. The write circuit used to program other configuration memories of the FPGA can be used to program PCCBs. As shown in Fig. 2, if any of the PCCBs is configured to value 1, the input and output crossbars will be enabled. Otherwise, the input and output crossbars will be power-gated. Furthermore, PCCBs control the power supply of the corresponding GRHL or LUT cells. Hence, by appropriately configuring PCCBs, one can enable only the used GRHL and LUT cell in the MC and disable the others. If none of the cells in the MC are utilized in a design, the value of all PCCBs of the MC can be configured to 0 to disable the entire MC.

III. Experimental Setup and Results

In this section, first the design process of GRHL cells for the proposed MC is discussed for a set of benchmark circuits. To this end, 20 largest MCNC benchmark circuits are

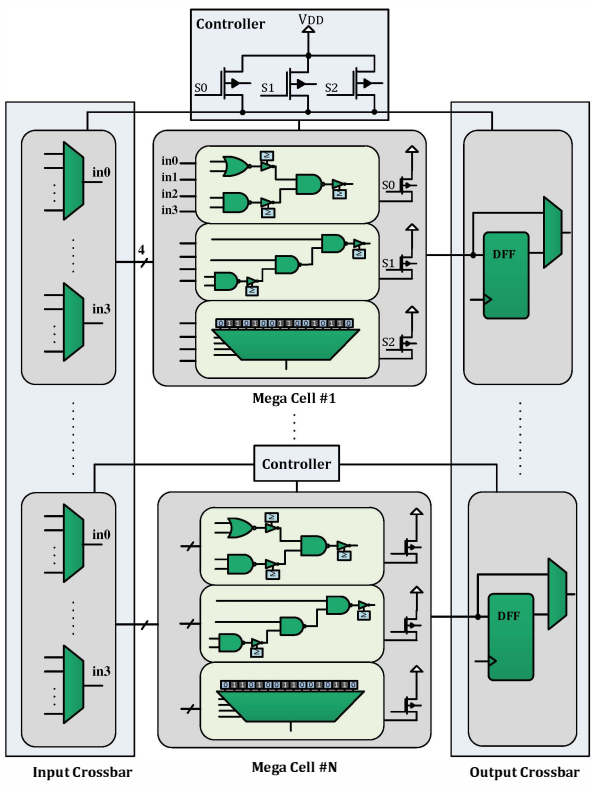


Fig. 2. The overall structure of the MCs

TABLE I. Coverage ratio of 4-input NPN classes in 20 largest MCNC benchmark circuits

NPN class	Ratio	GRHL1	GRHL2
ABCD	39.9%	✓	
A(B+CD)	18.2%		✓
AB(C+D)	16.6%	✓	
AB+CD	9.4%	✓	
A(B+C+D)	9.8%		✓
Others	6.0%		
Total	100%	66.0%	28.0%

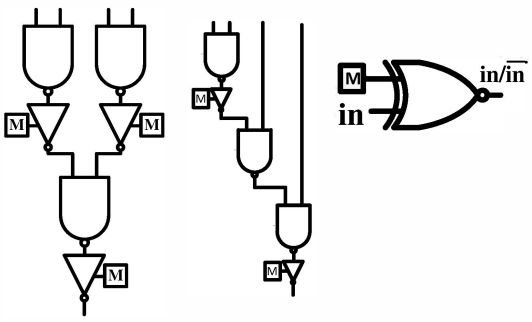
selected. Furthermore, the process of mapping to the MCs is described. Next, the experimental setup and the architectural parameters used in our experiments are presented. Then, the implementation and the evaluation flow is detailed. We also provide a detailed comparison between the proposed MC-based architecture and baseline architectures including LUT-(4 and 6)-based architectures and *Fine-Grained Power Gated* (FGPG) architecture [15].

A. Proposed GRHLs

In order to design GRHLs, the occurrence frequency of NPN classes is studied in the benchmark applications. Implementing the most frequent NPN classes by the GRHLs will lead to a high P_{GRHLs}. According to Equation 1, this will make the MC more power-efficient. Table I presents the coverage ratio of 4-input NPN classes in the benchmark applications. In order to extract these results, 20 largest MCNC benchmark circuits mapped to LUT-4 cells by ABC [19]. Then, the occurrence frequencies of NPN classes are extracted by the means of *Boolean Matcher* [20]. As shown in Table I, more than 94% of 4-input functions belong to one of the five most frequent NPN classes presented in Table I. Having the design constraints mentioned in Sec. II-B, two GRHLs named GRHL1 and GRHL2 are proposed. Fig. 3(a) and Fig. 3(b) show the proposed GRHL1 and GRHL2 cells, respectively. The proposed GRHLs are designed to implement the five most frequent NPN classes demonstrated in Table I. Configurable inverters inside the proposed GRHLs provide the ability to implement multiple NPN classes. Therefore, the coverage ratio of GRHLs (and consequently P_{GRHLs}) will be more than 94%. The proposed GRHLs are designed heuristically to cover the five most frequently NPN classes.

Although GRHL2 covers only 28.0% of functions, it covers NPN classes which are not covered by GRHL1. Note that there is no intersection between the covered functions of GRHL1 and GRHL2. The union of GRHL1 and GRHL2 cells (i.e, GRHL1 $\cup$ GRHL2) can cover more than 94% of functions with minimal power overheads. Three and two configurable inverters are employed in GRHL1 and GRHL2, respectively. The configurable inverter which is demonstrated in Fig. 3(c), propagates either the original input signal or its inverted form based on the value of its SRAM configuration memory.

Note that inputs permutation is possible through configurable routing network in FPGAs. The negation of outputs is also provided by the means of configurable inverter placed at the output of both GRHL1 and GRHL2. However, for negating inputs, unlike macro-gate [14], no configurable inverter is employed at the inputs of GRHLs. Instead, the negation of



(a) GRHL1 (b) GRHL2 (c) Config. Inverter

Fig. 3. Proposed GRHLs and configurable inverter

TABLE II. CHARACTERISTICS OF THE PROPOSED GRHLS VS. CONVENTIONAL LUTS

Logic Cell	Delay (ps)	Power(μW)		# SRAMs
		Static	Dynamic	
GRHL1	60.3	0.43	0.10	3
GRHL2	73.6	0.32	0.04	2
LUT-4	84.5	1.37	0.34	16
LUT-6	243.0	5.66	0.84	64

inputs is fast forwarded to the next stage. Note that in the technology mapping step, a negation can be implemented by either the current stage or the next stage. Hence, in the presence of multiple fanout where both true and inverted forms are required or when only the inverted form is required, the negation can be fast forwarded to the next stage. This imposes a marginal complexity to the technology mapping step. However, based on our experiments, it imposes less power overheads as compared to conservatively adding configurable inverters to each input line of GRHLs. Table II summarizes the characteristics of the proposed GRHLs as compared to the conventional LUTs, extracted by HSPICE simulations using 45nm library.

B. Mapping to MCs

Fig. 4 illustrates the overall flow of function mapping to the proposed MC-based architecture. First, the blif file of each circuit is mapped to the soft logic architecture (LUT-4) by ABC [19]. This shrinks the circuit to 4-input functions which are mapped to LUT-4 cells. Next, the NPN classes of each function is extracted by the means of Boolean Matcher. Lastly, the circuits which are already mapped to the LUT-4 cells are re-mapped to the MCs. Having the NPN class of each function (node) in the blif files and also the NPN classes supported by each GRHL, the nodes are mapped to the GRHLs. Then, if a node could not be implemented by neither GRHL1 nor GRHL2, it will remain as a LUT-4 cell. Therefore, each node which is formerly mapped to a LUT-4 cell will be mapped to either GRHLs or the LUT-4 cell in the MC. Hence, there exists a one-to-one mapping between each LUT-4 cell in the original blif files and the MCs in the final blif files. To handle the situations where the GRHLs in the MC support common NPN classes, the priority of mapping is set to the GRHL cell with less power consumption.

C. Architectural Parameters

Table IV reports the architectural parameters of both the proposed and the baseline architectures used in the experiments. The abbreviations used in this table has been defined in Table III. Same as the most of the state of-the-art FPGAs, a depopulated cluster is used for both the proposed and the baseline architectures. In order to achieve an efficient depopulated implementation, the architectural parameters reported in [21] are used for both the proposed and the baseline architectures.

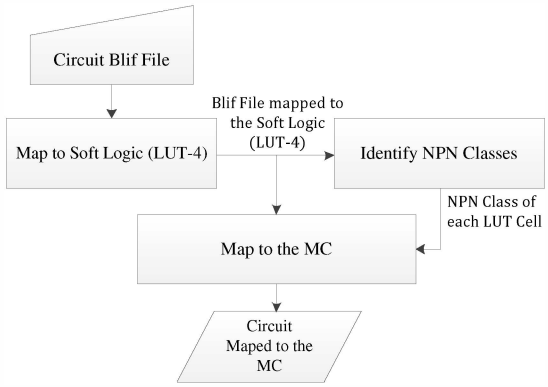


Fig. 4. Overall Mapping Flow of Soft Logic to Mega Cells

D. Experimental Setup and Evaluation

Both the proposed and baseline architectures are composed at circuit-level netlist and simulated in HSPICE to extract the performance and power results. For the case of LUT-4 and LUT-6, we used pass-gate based multiplexer to further improve their performance and power consumption. All of the power gating PMOS transistors are sized as 20X to deliver appropriate voltage level. However, this causes an average of 14% LB delay overhead for both the FGPG and proposed architecture. Better performance results can be achieved at the cost of more power gating area overhead. In addition, the configuration of LBs, *Switch Boxes* (SBs), and *Connection Blocks* (CBs) are extracted from the VPR [22] simulation reports and then imported to the HSPICE simulations. In the experiments, we have explored the technology trends for both the proposed and baseline architectures. To this end, cell libraries of 65, 45, and $32nm$ for an optimum value are obtained from [23] suite and imported to the HSPICE simulations. Finally, the delay, power, and *Power Delay Product* (PDP) results are extracted from HSPICE reports for 20 largest MCNC benchmark circuits. For brevity, here we only report the average of delay, power, and PDP results over these benchmark circuits.

E. Critical Path Delay

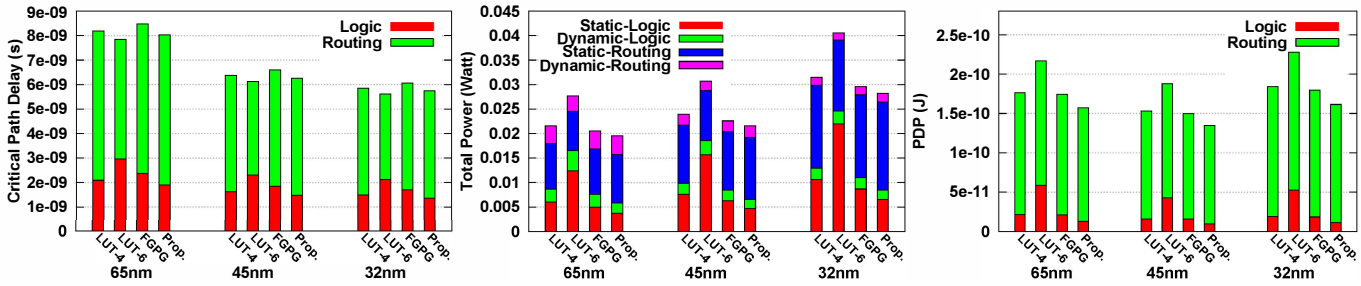
Fig. 5(a) illustrates the critical path delay of the proposed architecture as compared to the baseline architectures in terms of logic and routing delays. According to Table II, the proposed

TABLE III. PARAMETERS DEFINITION

N: Cluster size K: LUT size	F_c: Routing channel to cluster input density
I: Number of cluster inputs	I_{spare}: Number of additional cluster inputs
F_{cin} : I to K ratio	F_{cfb}: LUT feedback to K ratio

TABLE IV. ARCHITECTURAL PARAMETERS

Parameter	Proposed	LUT-4	LUT-6	FGPG [15]
N	6	6	6	6
K	4	4	6	4
I	14	14	21	14
F_c	0.5	0.5	0.5	0.5
I_{spare}	2	2	2	2
F_{cin}	0.5	0.5	0.33	0.5
F_{cfb}	0.5	0.5	0.5	0.5



(a) Critical Path Delay. (b) Total Power. (c) Power-Delay Product.

Fig. 5. Proposed Architecture vs. Baseline Architectures

GRHLs in the MC have much less propagation delay compared to LUT-4/6. However, in contrast to the LUTs, they do not support input permutation. This imposes further overheads and pressure on the global routing in the proposed architecture as compared to the baselines. As a result, the proposed architecture reduces the logic delay on average by 9.0%, 35.8%, and 20.0%, as compared to LUT-4, LUT-6, and FGPG architectures, respectively. Nonetheless, the total performance improvements are only 2.0% and 5.3% as compared to the LUT-4 and FGPG architectures, respectively. The critical path delay is even slightly increased in the proposed architecture as compared to the LUT-6 based architecture by 2.3%

Unlike the proposed architecture, the FGPG architecture does not make any improvement over the critical path delay and even worsens the performance as compared to the LUT-4 based architecture. This is due to the fact that the FGPG architecture proposed in [15] only applies power gating to the unused LUTs and does not make any improvement over the critical path. Moreover, as explained in Sec. III-D, due to the performance overhead caused by the voltage drop in the power gating transistors, the FGPG imposes further performance overheads.

F. Power

As shown in Fig. 5(b), the proposed architecture reduces the logic power consumption by 32.6%, 33.6%, and 34.6% in 65, 45, and 32nm technologies, respectively, as compared to the LUT-4 based FPGA. In addition, the logic power consumption is reduced in the proposed architecture by 64.5%, 64.9%, and 65.6% in 65, 45, and 32nm technologies, respectively, as compared to the LUT-6 based FPGA. Hence, the power saving of the proposed architecture is more pronounced with technology scaling. As shown in Fig. 5(b), the logic power consumption improvements of the proposed architecture as compared to FGPG in the various technology nodes is approximately 23.0%. This indicates that not only the power consumption of unused LUTs is a serious concern but also the power consumption of used LUTs is important.

As it was expected due to the overheads of global routing, the overall power efficiency of the proposed architecture is not as high as the logic power improvement. Nevertheless, the proposed architecture reduces the total power consumption up to 10.4% as compared to the LUT-4 based FPGA. In addition, the total power consumption is reduced in the proposed architecture by 29.2%, 29.7%, and 30.4% in 65, 45, and 32nm technologies, respectively, as compared to the LUT-6 based FPGA. Furthermore, the proposed architecture shows on average 4.6% higher power efficiency as compared to the FGPG architecture.

TABLE V. NORMALIZED AVERAGE TOTAL AREA OF 20 LARGEST MCNC BENCHMARK CIRCUITS

Architecture	LUT-4	LUT-6	FGPG	Prop.
Normalized Area	1.00	1.32	1.02	1.17

G. Power-Delay Product

Fig. 5(c) illustrates the PDP of the proposed architecture as compared to the baselines in terms of logic and routing PDP. Since the proposed architecture improves both the performance and the power consumption of logic cells, a significant logic PDP reduction is achieved by 39.5%, 39.6%, and 40.7% in 65, 45, and 32nm technologies, respectively, as compared to the LUT-4 based FPGA. In addition, the proposed architecture reduces the logic PDP up to by 38.7% as compared to the FGPG. Lastly, as compared to the LUT-6 based architecture logic PDP is reduced in the proposed architecture by 77.9%, 77.4%, and 78.4% in 65, 45 and 32nm technologies, respectively.

Same as the logic PDP improvements, the proposed architecture improves the total PDP. The proposed architecture reduces the total PDP up to 12.1%, 28.8%, and 9.6% as compared to the LUT-4, LUT-6, FGPG based architectures, respectively. The overall PDP and energy consumption efficiency of the proposed architecture can improve the run-time of the FPGAs in the battery powered devices. This can make FPGAs a more attractive platform for mobile devices.

IV. LIMITATIONS

As shown in Sec. III, the proposed MC achieves considerable energy improvements over the LUT-based and the FGPG architectures. However, the proposed MC comes with several limitations. First, the proposed GRHLs used in the experiments are tuned for a set of benchmark applications. As a result, it can be expected that their coverage ratio and effectiveness will be different for other applications. This is due to the reduction in the flexibility of GRHLs which on the one hand, increases the power efficiency of the GRHLs, but on the other hand limits the coverage ratio of the GRHLs for various applications. However, FPGA vendors usually offer various series for different application domains. Therefore, GRHLs in the MC can be optimized for each application domain to achieve higher efficiency.

Another limitation of the current work is its area overheads. Table V demonstrates the normalized average total area of the 20 largest MCNC benchmark circuits for the proposed architecture and the baselines. The total area is calculated as the sum of the total minimum width transistors of LBs and SBs, including all the configuration memory cells and power gating transistors. Note that due to limitations of VPR toolset, the impact of CLB area increase on the total wire length and routing area is not considered neither for the

proposed architecture nor for the baseline FGPG and LUT-based architectures. However, for the proposed architecture its impact would be limited due to low overheads of the GRHLs and the PCCB. All of the results are normalized to the LUT-4 based architecture area. The proposed MC, on average, imposes an area overhead of 17.4% as compared to the LUT-4 based architecture, however, it reduces the total area by 11.6% as compared to the LUT-6 based architecture. Note that in the dark silicon era where the power efficiency is the main design paradigm, such area overheads are justified.

Finally, the scalability of the proposed MC for the MC input sizes larger than four ($K > 4$) is challenging. As discussed earlier in Sec II, the main difficulty in scaling of the MC is finding a small subset of GRHLs to cover a high ratio of NPN classes for more than 4-input logic functions. However, the proposed 4-input MC achieves almost the same performance efficiency as the LUT-6 based FPGA which is highly used in the state-of-the-art FPGAs. In addition, the proposed MC improves the power consumption and the PDP as compared to the LUT-6 based architecture up to 30.4% and 28.8%, respectively. Note that as mentioned in [17], scaling K to larger values than six does not lead to performance improvements and K=6 provides the best performance efficiency. Therefore, although the proposed MC suffers from scalability issues for larger values of K, it offers better power efficiency with almost same performance as the optimum LUT-based architecture.

V. Conclusion and Future Work

In this paper, we proposed a power-efficient *Mega Cell* to reduce the power consumption of FPGAs in the dark silicon era. The proposed MC consists of a set of GRHLs, an LUT, and power-controlling configuration bits, called PCCBs. The proposed MC is designed in a way which at most one cell in the MC is active and the other cells are power gated. The proposed MC not only reduces the static power consumption of unused resources but also improves power and performance efficiency of the used resources. The results indicate that the proposed MC-based architecture can improve logic performance, power, and PDP up to 35.8%, 65.6%, and 78.4%, respectively, as compared to the equivalent LUT-based architecture.

Our experiments show that if we exploit low-power SRAM technology instead of conventional SRAM technology in configuration bits of both the baseline and proposed architecture, the PDP improvement will be reduced to 6%. Therefore, in our future work we plan to replace the LUT cell in the MC with the multiple cascaded GRHLs. So in case a function could not be mapped to any of the GRHLs, it will be implemented by cascading multiple GRHLs in different MCs.

References

[1] M. B. Taylor, "Is dark silicon useful?: Harnessing the four horsemen of the coming dark silicon apocalypse," in *Proceedings of the 49th Design Automation Conference*. ACM, 2012, pp. 1131–1136.

[2] M. Taylor, "A landscape of the new dark silicon design regime," *IEEE Micro*, vol. 33, no. 5, pp. 8–19, 2013.

[3] C. Maxfield. (2011) Xilinx announces worlds highest capacity fpga. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1260468

[4] I. Kuon and J. Rose, "Measuring the gap between fpgas and asics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 2, pp. 203–215, 2007.

[5] C. H. Hoo, Y. Ha, and A. Kumar, "A directional coarse-grained power gated fpga switch box and power gating aware routing algorithm," in *Proceedings of the 23rd International Conference on Field-Programmable Logic and Applications*, 2013, pp. 1–4.

[6] Altera, "Stratix iv device handbook," http://www.altera.com/literature/hb/stratix-iv/stx4_siv51004.pdf, 2012, vol.1 Chap.4.

[7] Xilinx, "Virtex-6 fpga configurable logic block," http://www.xilinx.com/support/documentation/user_guides/ug364.pdf, 2012, uG364(v1.2).

[8] P. Jamieson and J. Rose, "Enhancing the area-efficiency of fpgas with hard circuits using shadow clusters," in *Proceedings of IEEE International Conference on Field Programmable Technology*, 2006, pp. 1–8.

[9] H. Parandeh-Afshar, G. Zgheib, D. Novo, M. Purnaprajna, and P. Ienne, "Shadow aics: reaping the benefits of and-inverter cones with minimal architectural impact," in *Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays*, 2013, pp. 279–279.

[10] J. H. Anderson and Q. Wang, "Area-efficient fpga logic elements: Architecture and synthesis," in *Proceedings of the 16th. Asia and South Pacific Design Automation Conference*, ser. ASP-DAC '11. IEEE Press, 2011, pp. 369–375.

[11] ——, "Improving logic density through synthesis-inspired architecture," in *Proceedings of the 19th. International Conference on Field Programmable Logic and Applications*. IEEE, 2009, pp. 105–111.

[12] Y. Okamoto, Y. Ichinomiya, M. Amagasaki, M. Iida, and T. Sueyoshi, "Cogre: A configuration memory reduced reconfigurable logic cell architecture for area minimization," in *Proceedings of the 20th International Conference on Field Programmable Logic and Applications*. IEEE, 2010, pp. 304–309.

[13] H. Parandeh-Afshar, H. Benbihi, D. Novo, and P. Ienne, "Rethinking fpgas: elude the flexibility excess of luts with and-inverter cones," in *Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*. ACM, 2012, pp. 119–128.

[14] Y. Hu, S. Das, S. Trimberger, and L. He, "Design and synthesis of programmable logic block with mixed lut and macrogate," *Transactions on Computer-Aided Design and Integrated Circuits and Systems*, vol. 28, no. 4, pp. 591–595, Apr. 2009.

[15] S. Ishihara, M. Hariyama, and M. Kameyama, "A low-power fpga based on autonomous fine-grain power gating," *Very Large Scale Integration (TVLSI) Systems, IEEE Transactions on*, vol. 19, no. 8, pp. 1394–1406, 2011.

[16] A. A. Bsoul and S. J. Wilton, "An fpga architecture supporting dynamically controlled power gating," in *Proceedings of the International Conference on Field-Programmable Technology*, ser. FPT'10. IEEE, 2010, pp. 1–8.

[17] E. Ahmed and J. Rose, "The effect of lut and cluster size on deep-submicron fpga performance and density," *Very Large Scale Integration (TVLSI) Systems, IEEE Transactions on*, vol. 12, no. 3, pp. 288–298, 2004.

[18] A. A. Kennings, K. Vorwerk, and A. Mishchenko, *Generating efficient libraries for use in FPGA resynthesis algorithms*. Department of Electrical and Computer Engineering, University of Waterloo, 2010.

[19] BLSG, "Abc: A system for sequential synthesis and verification," *Berkeley Logic Synthesis and Verification Group*, 2011.

[20] D. Chai and A. Kuehlmann, "Building a better boolean matcher and symmetry detector," in *Proceedings of the conference on Design, automation and test in Europe*. European Design and Automation Association, 2006, pp. 1079–1084.

[21] G. Lemieux and D. Lewis, "Using sparse crossbars within lut," in *Proceedings of the ACM/SIGDA ninth international symposium on Field programmable gate arrays*, 2001, pp. 59–68.

[22] J. Rose, J. Luu, C. W. Yu, O. Densmore, J. Goeders, A. Somerville, K. B. Kent, P. Jamieson, and J. Anderson, "The vtr project: architecture and cad for fpgas from verilog to routing," in *Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*. ACM, 2012, pp. 77–86.

[23] (2013) Predictive technology model (ptm). [Online]. Available: http://ptm.asu.edu/