

VTR

A brief introduction to VTR

Data Storage Networks(DSN)

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Features

- Benchmarks consisting of real applications that contain both memories and multipliers.
- Packing/Clustering support for FPGA logic blocks with widely varying functionality
- A front-end Verilog elaborator that has support for hard blocks.
- The flow is currently area-driven. We are currently working on adding timing information back into the CAD flow.

Flow

Input:

- User circuit
 - Verilog
 - Blif
- FPGA architecture
 - FPGA architecture description language
- Output:
 - placed-and-routed FPGA.

Installing

- Could be installed in
 - Linux
 - Cygwin
- Make problems
 - Package dependencies
 - /bin/sh: ctags: not found
 - apt-get install exuberant-ctags
 - Libraries
 - /usr/bin/ld: cannot find -ltermcap
 - sudo apt-file update
 - apt-file search libtermcap.so
 - Install the appropriate dev package

A sample test

- Make test
- run_quick_test.pl

```
run_quick_test.pl: command not found
ali@ali-N82JQ:~/vtr_release$ ./run_quick_test.pl
=====
Test Verilog-to-Routing Build Infrastructure
=====

Testing ODIN II: [PASSED]

Testing ABC: [PASSED]

Testing VPR: [PASSED]

Test complete
ali@ali-N82JQ:~/vtr_release$
```

A benchmark

- Set env_variable in .bashrc

```
~/.bashrc: executed by bash(1) for non-login shells.  
# see /usr/share/doc/bash/examples/startup-files (in the package bash-doc)  
# for examples  
export REGRESSION_BASE_DIR=/home/ali/vtr_release/reg_test
```

- Run test scripts

```
ali@ali-N82JQ:~/vtr_release/reg_test/TESTS$ ./SCRIPTS/run_reg_tests.pl small_reg_test.txt local >& out.txt  
ali@ali-N82JQ:~/vtr_release/reg_test/TESTS$ ./SCRIPTS/parse_reg_tests.pl small_reg_test.txt  
ali@ali-N82JQ:~/vtr_release/reg_test/TESTS$ more reg_test_results.txt  
Regression Test  
Test case sample_test_1:  
[Fail] k6_N8_memSize32768_memData32.xml-ch_intrinsics.v route_time: test = 1.16 golden = 3.81  
[Fail] k6_N8_memSize32768_memData32.xml-diffeq1.v route_time: test = 10.74 golden = 5.93
```