A Layout-based Approach for Multiple Event Transient Analysis

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ABSTRACT

With the emerging nanoscale CMOS technology, *Multiple Event Transients* (METs) originated from radiation strikes are expected to become more frequent than *Single Event Transients* (SETs). In this paper, a fast and accurate layout-based *Soft Error Rate* (SER) estimation technique with consideration of both SET and MET fault models is proposed. Unlike previous techniques in which the adjacent MET sites are obtained from logic-level netlist, we perform a comprehensive layout analysis to extract MET adjacent cells. It is shown that layout-based technique is the only effective solution for identification of adjacent cells as netlist-based techniques significantly underestimate the overall SER.

Categories and Subject Descriptors

B.8.1 [**Reliability, Testing, and Fault-Tolerance**]

General Terms

Reliability

Keywords

Transient errors, Soft errors, Error propagation

1. INTRODUCTION

By downscaling of transistor feature size and operating voltage together with increased device count per chip, the susceptibility of circuits to soft errors has significantly increased in the past years [1, 2]. In the absence of protection mechanisms, the system *Soft Error Rate* (SER) will grow in direct proportion to the number of cells in the design [2, 3].

Transient errors caused by a single particle strike in combinational gates and sequential elements (i.e., memory cells, latches and flip-flops) are called *Single Event Transient* (SET) and *Single Event Upset* (SEU), respectively. SET and SEU fault models have been widely studied over the recent years [4, 5, 6, 7, 8, 9]. With smaller device geometries in nanoscale technologies, it is very likely that a high energy particle strike affects several adjacent cells in a circuit resulting in *Multiple Event Transients* (MET) in combinational gates or *Multiple Bit Upsets* (MBU) in sequential elements [10, 11, 12, 13].

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In previous technology nodes, soft errors had a considerable effect only in sequential elements which were significantly mitigated by means of *Error Correcting Codes* (ECCs) [14, 15, 16] and built-in soft error tolerance [17, 18, 19, 20]. Recent experiments reveal that the contribution of combinational gates is considerable in nanoscale technologies [21, 22]. Furthermore, it is claimed that a remarkable fraction of particle strikes results in MET [13, 23]. In order to cost-effectively mitigate soft errors in the presence of both SETs and METs, their impacts at the layout and logic levels must be accurately modeled.

The analytical techniques presented in [24] and [25] address the MET fault model in logic circuits. The *Error Probability Propagation* (EPP)-based technique presented in [24] propagates the error probabilities from the error sites towards primary outputs and sequential elements. The technique presented in [25] is based on *Boolean Decision Diagrams* (BDDs) and provides more accuracy at the expense of runtime, compared to the earlier method [7]. The major shortcoming of these techniques in estimating SER due to METs is that they use logic-level netlist for identification of MET error sites, neglecting layout-level adjacency of error sites. Such assumption can significantly underestimate the circuit SER as we will experimentally demonstrate later in this paper. Additionally, the distribution of affected error sites and the number of affected cells completely depends on the layout-level details and cannot be extracted from the netlist. For example, our experiments show that a considerable fraction of particles simultaneously affects both combinational gates and flip-flops, which is completely ignored in previous techniques. Ignoring such cases can further increase the SER inaccuracy. In this paper, occurrence of multiple transient errors at sequential elements, combinational gates, or combination of them is called *Multiple Transients* (MT).

In this paper, a fast and accurate technique is proposed for SER estimation considering the effect of MTs at the circuit layout. In the proposed technique, the surface affected by a particle in combinational and sequential logic is estimated with oval shapes obtained from available MBU patterns in memory arrays. Considering MBU patterns occurrence probability, ovals are randomly placed at different locations inside the circuit and the list of affected cells are extracted. Then, logic level analysis with multiple error propagation is performed to obtain the overall SER. Analysis of ISCAS'89 and ITC'99 benchmark circuits reveal that less than 10% of the netlist adjacent cells are physically adjacent in the layout. Also, more than 60% of physically adjacent cells are not adjacent in the netlist. Experimental results show

that neglecting layout adjacency can cause inaccuracy up to 36.04% in the circuit overall SER.

The rest of this paper is organized as follows: Section 2 motivates for layout-based MT modeling and investigates the validity of the netlist-based adjacency assumption used in previous techniques. In Section 3, the proposed layout-based approach is explained. Section 4 demonstrates the experimental results, and finally, the conclusion is given in Section 5.

2. MOTIVATION FOR LAYOUT-BASED MT ANALYSIS

An important step in MT analysis is identifying physically adjacent cells as error sites. Although, the layout of the circuit is necessary for accurate identification of adjacent cells, the previous MT analysis techniques presented in [24] and [25] employ some heuristic approaches to extract the list of adjacent cells from the netlist. In these techniques, four categories including a gate and its fan-in (GFI), a gate and its fan-out (GFO), common fan-ins of a gate (CFI), and common fan-out of a gate (CFO) are considered as adjacent nodes for MT error sites. Fig. 1 shows several examples of netlist-based adjacencies. In these techniques, a gate is first selected as primary error site and then its MT pair is randomly selected among its netlist adjacent cells.

In order to check the accuracy and layout-relevance of this model, i.e., extraction of adjacent cells from the logic netlist, the layout of several circuits selected from ISCAS'89 and ITC'99 benchmarks have been comprehensively analyzed (the details of this analysis framework is provided in Section 4). In this regard, all possible adjacency pairs for different netlist adjacency categories are first extracted from the netlist and then the physical adjacency of each pair in the circuit layout is investigated. Since the order of adjacency pairs is not important in this investigation, both GFI and GFO categories are equal and are assumed as a single category called GFI/GFO. In the example given in Figure 1, E is the fanout of gate B and gate B is a fanin of gate E. As result, pair (B,E) belongs to both GFI and GFO categories. Figure 2 shows the results of this experiment. As it can be seen, on average, only less than 10% of netlist adjacent pairs are also adjacent in the circuit layout. Also, the probability of physical adjacency of GFI/GFO category is much higher than that of CFI and CFO categories.

There is another experiment conducted in which all layout adjacencies on the circuit layout are first extracted and then for each physical adjacency, its netlist adjacency category is investigated (Figure 3). It can be inferred from Figure 3 that more than 60% of the physical adjacencies do not belong to the previously defined netlist adjacency categories.

From these two experiments, it becomes clear that there is no statistically meaningful correlation between netlist and

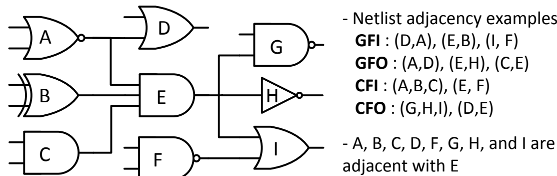

Figure 1: Examples of different adjacency scenarios considered in the netlist

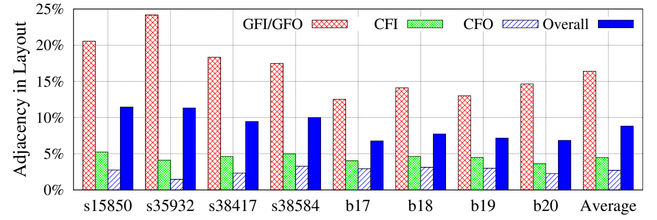

Figure 2: Relevance of different adjacency scenarios considered in the netlist to layout adjacency

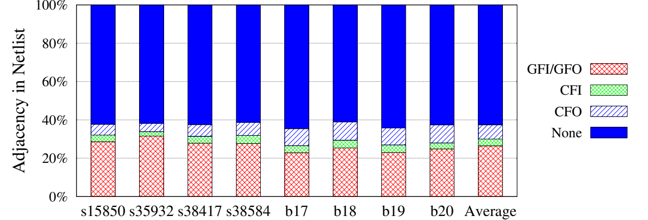

Figure 3: Relevance of extracted adjacencies from layout to netlist-level MT error models

layout adjacencies. This means that for accurate MT analysis, netlist-level analysis and MT error site abstraction is not sufficient and layout-level analysis must be performed. To address this issue, we propose a fast and accurate layout-based MT modeling technique and then the computed layout-based SERs are compared with the SERs obtained by the previously proposed netlist-based techniques.

3. PROPOSED LAYOUT-BASED MT MODELING

In this section, the proposed layout-based SER estimation approach with consideration of MT fault model is explained. This approach has two main steps, layout-based MT error site extraction and multiple error propagation at logic-level.

3.1 Layout-based MT Error Site Extraction

3.1.1 MT Error Site Extraction Using MBU Analysis

The first step for accurate MT modeling is extracting physically adjacent error sites from the circuit layout. This requires to have MT patterns projected in the circuit layout and their occurrence probability. However, due to the observation limits of logic, especially combinational blocks, and their irregularity as compared to memory arrays (such as SRAMs), to the best of our knowledge, no field results about MT patterns on combinational and sequential logic has been reported in the literature. Since memory arrays are much more regular and dense than logic structures and also have a full observability, the affected area can be accurately estimated. In this work, we try to use available MBU patterns in memory arrays for identification of MT error sites in logic circuits. In this method, the surface affected by a strike in a memory array is first extracted and then all logic cells covered by a similar surface are assumed to be MT error sites.

For this purpose, the affected area for each MBU pattern is first extracted. Predominant MBU patterns in memory arrays have been comprehensively studied using neutron beam-based accelerated SER estimation [10, 11]. The num-

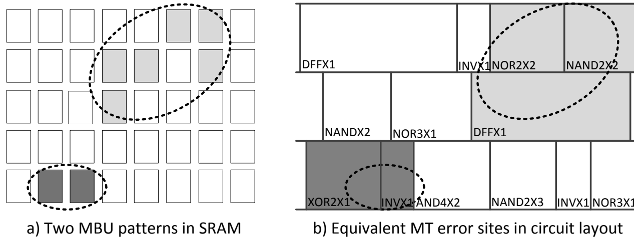

Figure 4: Extraction of MT error sites from existing MBU patterns

ber of affected bits by a single strike depends on several parameters including particle type and its energy, strike angle, cell type, cell size, and output load [12]. Given memory cell dimension as well as vertical and horizontal distance between adjacent cells, for each MBU pattern the surface affected by the strike can be calculated. Most of the MBU patterns, especially MBUs with more than eight bits, can be effectively covered by an oval surface. As a result, in our approach as shown in Figure 4, all cells affected by an MBU are first surrounded by an oval. Then, during SER estimation the same oval is transferred to random locations inside the logic layout and all cells affected by the MT are listed as error sites.

3.1.2 Library Characterization

In the circuit layout, only a subset of cells which have an overlap with the oval surface are considered as error sites. A cell has overlap with an oval surface if at least one of the *sensitive zones* to soft errors (N-diffusion and P-diffusion) falls within the surface. In fact, when a particle strikes a cell, it causes the additional charge to be collected in the diffusion parts of the transistor which in turn disturbs the normal operation of the transistor. The charge collected to the diffusion parts which are connected to VDD and GND pins is evacuated and does not affect the circuit behaviour. The other parts of the diffusion can be disturbed by collection of additional charge. Figure 5 shows how sensitive zones for a NAND gate layout are extracted based on this explanation. Using this approach, all cells inside the technology library are characterized and sensitive zones coordinations are extracted.

3.1.3 Overall Flow

The main steps of the proposed layout-based SER estimation are summarized in Algorithm 1. Initially, the list

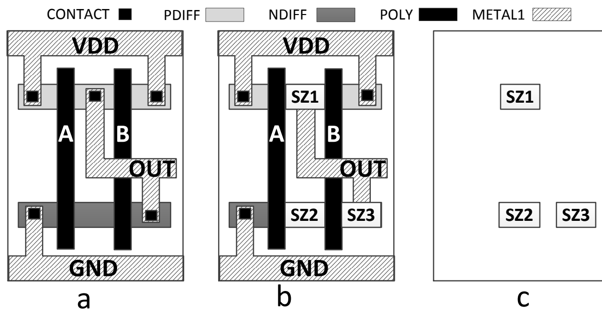

Figure 5: Sensitive Zone (SZ) extraction for a NAND gate: a) cell layout b) identification of diffusion parts which are not connected to supply voltage c) sensitive zones (adapted from [26])

Algorithm 1: Layout-based SER estimation

1 Extract a surrounding oval for each MBU pattern
2 Extract sensitive zones of each cell by library characterization
3 Divide layout into smaller grids and extract the list of cells in each grid
4 **while** *sampling error < predefined value AND number of cells covered by at least one MT < 99.9%* **do**
5 | Randomly select an oval based on their occurrence probability
6 | Place the oval in a random location on the layout
7 | Find the list of grids which have overlap with the oval
8 | Search overlapped grids cell lists and construct overlapped cells list
9 | Remove cells without overlapped sensitive zones from cell list
10 | Mark all cells in overlapped cell list as covered by an MT
11 | Propagate MT at logic-level and calculate failure probability
12 **end**
13 Report average failure probability

of ovals and their occurrence probability are extracted from existing MBU patterns (line 1) and then technology library is characterized for identification of sensitive zones (line 2). These two steps are performed once in advance and their results are used for all circuits to be analyzed in the same technology and library settings.

Due to large number of cells and sensitive zones inside industrial-size circuits, a hierarchical approach is employed to minimize the time needed for identification of error sites affected by an MT (line 3). In this approach, the entire layout area is divided into smaller grids and the list of cells inside each grid is extracted. During SER estimation, instead of searching among large number of cells, in the first step, for each grid it is checked whether it has an overlap with the oval surface and the list of layout grids overlapped by the oval surface is extracted. Then, the list of overlapped cells is extracted by investigation of cells inside overlapped layout grids. At the end, those cells which have no overlapping sensitive zone with the oval surface are eliminated from the target cell list. The remaining cells will be used as candidate MT fault sites (line 7-9).

3.2 Multiple Error Propagation

In the layout-based MT error sites extraction, it is quite possible that flips-flops and combinational gates are simultaneously affected by an MT. This issue is completely ignored in the previous work. In such scenarios, a transient pulse is produced at the output of affected cells while the value stored in flip-flops are logically inverted. To handle such cases, a fast and accurate propagation mechanism is required.

During multiple error propagation, unified treatment of three timing masking factors, i.e. logical, electrical, and latching-window, is essential for accurate SER estimation [7, 4]. The four-value logic (0, 1, 0^e, 1^e) [24] which offers an effective trade-off between runtime and accuracy, is employed to compute the logical masking factor. This technique can efficiently handle the effect of single error propagation in re-convergent paths as well as the effect of multiple errors propagation in convergent paths. For electrical masking factor, the equation-based transfer function presented in [27] is adopted. This techniques models a transient pulse using a trapezoidal model and can accurately compute the electrical attenuation. Latching-window masking model is based on the well-known and widely used equation presented in [28].

It is quite possible that an MT does not propagate to the primary outputs in the first cycle, rather it may latched in some flip-flops and propagates to the primary outputs in the subsequent cycles. Experimental results in [29] reveal

that failure probability saturates in few cycles (normally less than 10 cycles) after error occurrence. Multi-cycle error propagation is also taken into account in our framework.

While propagating errors along combinational gates, all three masking factors should be considered in the first cycle. At the end of the first cycle, the error is captured in the flip-flops or eliminated (masked) from the system. In the subsequent cycles, only logical masking factor can prevent the error from propagation and as a result, the other masking factors are ignored. In contrast, when a strike affects a flip-flop, in all cycles including the first cycle, only logical masking is taken into account. In case of simultaneous error occurrence at both logic gates and flip-flops, all three masking factors have been considered in the first cycle. However, the width of the output transient pulse of erroneous flip-flops is set to be equal to the clock period to overcome the latching-window masking factor for such errors.

3.3 Combined Layout and Logic SER Analysis

Since there are lots of oval shapes and each oval can be placed in different locations of the circuit layout, there are infinite MT scenarios even for very small circuits. Therefore, we use a Monte-Carlo simulation-based approach to extract the overall SER of the circuit with respect to MT. In this approach, in each iteration, based on the MBU patterns occurrence probability, one of them is randomly selected and its corresponding oval will be placed in a random location on the layout. After extracting the list of affected cells using the hierarchical approach, the errors are propagated from the error site and the failure probability for this MT is calculated. This continues until reaching a predefined accuracy level. An equation to compute the sampling error of Monte-Carlo simulations with respect to the number of iterations and current failure probability is provided in [30]. The MT analysis terminates when the sampling error is less than the predefined value and the number of cells contributed by at least one MT exceeds 99.9%. The second condition is used to become sure that most of the cells in the layout has been considered during SER estimation.

4. EXPERIMENTAL RESULTS

Using the proposed layout-based MT error site extraction and combined combinational and sequential multiple error propagation at logic-level, we have performed an extensive analysis on the impact of particle energy on the MT error sites. Also, the impact of netlist adjacency assumption on the overall SER of the circuit is investigated.

4.1 Work Flow

In order to show the scalability of the proposed approach, we have evaluated largest available benchmark circuits in ISCAS'89 and ITC'99 benchmarks suites. For each benchmark, the HDL description of the circuit is first synthesized using a Synopsis Design Compiler [31] with respect to Nangate 45 nm library. Then the layout of the netlist is extracted using SoC Encounter [32]. In the experiments, the layout is divided into 30 × 30 μm^2 grids. Each grid includes around 800 cells.

The MBU patterns for particles with 22, 37, 95, and 144 Mev provided by [10] are used during the layout-based MT extraction. This information is given to our layout-based SER estimation to calculate the overall SER of the circuit according to Algorithm 1. In our framework, SER estimation analysis terminates when the maximum inaccuracy of the Monte-Carlo is less than 0.5%.

The failure in this paper defined according to [29] as the probability of propagation from error sites to primary outputs during first few cycles after error occurrence. The error is propagated for 10 cycles and during error propagation, all three masking factors have been considered.

4.2 MBU Patterns and MT Error Sites

As mentioned earlier, in order to extract MT error sites, the area affected by MBU patterns are first extracted and then a surrender oval for each MBU pattern is constructed. These ovals are used for identification of MT error sites. For this purpose, detailed information about different MBU patterns in a memory array is necessary for identification of MT error sites.

Radaelli et. al. [10] have reported a detailed information about predominant MBU patterns in a 150 nm technology SRAM device and their occurrence probability for particles with 22, 47, 95, and 144 Mev energy. Considering the SRAM cell dimensions, the area affected by each MBU surrounding oval can be accurately estimated. For these cases, the oval shapes and their occurrence probability (same as the occurrence probability of the corresponding MBU pattern) are computed. Table 1 shows the average area affected by each particle energy obtained by wighted averaging of oval surfaces based on their occurrence probability.

Particle Energy (Mev)	Average Affected Area (μm^2)
22	1.178
47	1.902
95	2.903
144	4.613

Table 1: Average area affected with different particle energies

The area affected by a particle strike is mostly a function of particle energy, while the strength of the transient pulse mostly depends on other parameters such as diffusion volume (width, length, depth) and load capacitance [2]. As a result, the affected area information acquired for a 150 nm SRAM technology can also be used for the logic area affected by a particle strike with the same energy in the 45 nm technology. Please note that although the affected area remains constant, however, due to the technology downscaling, the number of affected cells increases in smaller technologies.

By randomly locating these ovals on the circuit layout according to their occurrence probability, different combinations of affected combinational gates and flip-flops are extracted and identified as MT error sites. Figure 6 shows the occurrence probability of different gate/flip-flop combinations for particle strikes with 22, 47, 95, and 144 Mev energy. As it is expected, by increasing the particle strike energy, the occurrence probabilities of SET and SEU decreases significantly and MT becomes predominant. In previous netlist-based techniques, it is assumed that a particle strike leads to either MET on combinational logic or MBU on sequential cells. Also, the number and type of affected cells was a function of the particle energy not layout. However, the results shown in Figure 6 clearly indicate that 1) both combinational and sequential cells can be affected by a single particle strike. 2) the number, type, and combination of affected cells depend on the layout structure as well.

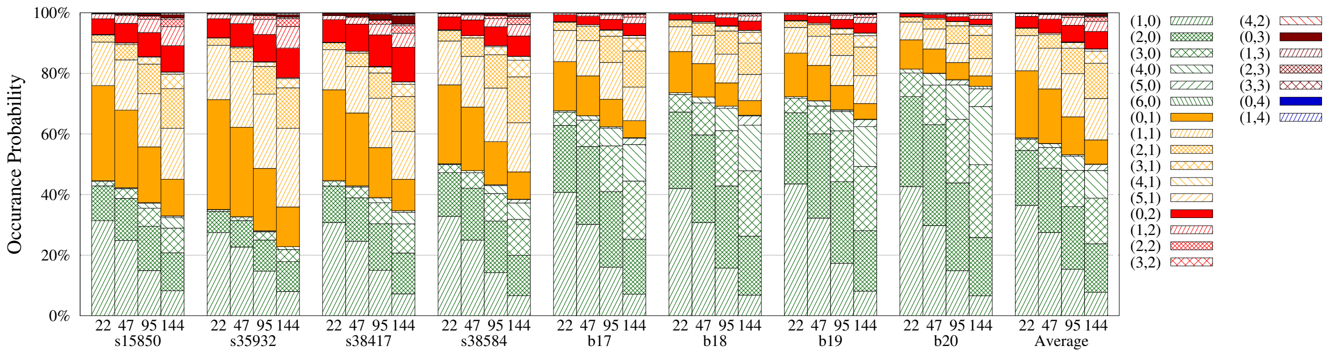

Figure 6: Different gate and flip-flops combinations affected by particle strikes with 22, 47, 95, and 144 Mev energy. For example, (3,2) means three gates and two flip-flops are affected by the particle

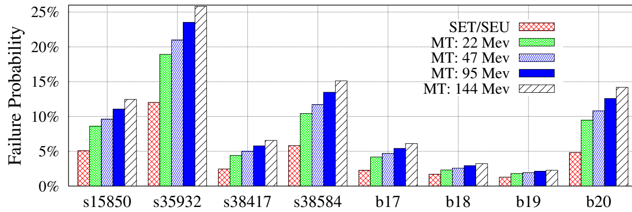

Figure 7: Failure probabilities for different particle energies

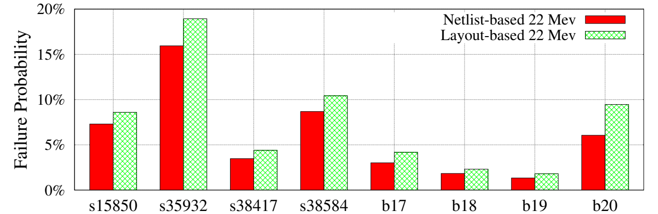

Figure 8: Comparison of overall SER obtained by netlist-based and layout-based approaches for particle with 22 Mev energy

4.3 Impact of SET/SEU Versus MT Model on Overall SER

In order to show the importance of MTs, overall SERs extracted for particles with 22, 47, 95, and 144 Mev energy are compared with the case that the simple SET/SEU model is considered (Figure 7). In case of SET/SEU, a single error is injected in each gate/flip-flop and the average of failure probabilities of all cells are reported as the circuit failure probability. All error sites are extracted from layout and propagated using the propagation method explained in Section 3.2. The results shown in Figure 7 also reveal that the circuit SER does not linearly increase with the particle energy. As an example, on average, the SER in the presence of 47 Mev particles is only 1.15X greater than when considering 22 Mev particles. This can be also explained by the number of affected cells for different particle energies reported in Figure 6.

4.4 Impact of netlist-adjacency assumption on SER

In order to investigate the effect of netlist adjacency on the overall SER, we have implemented a netlist-based approach. The error propagation method of the netlist-based approach is similar to the one explained in Section 3.2. Although different combinations of affected cells and their occurrence probability are unknown at the netlist-level, in order to have a fair comparison, the same occurrence probabilities is also used in the netlist-based approach. Figure 8 reports the failure probability obtained by both netlist- and layout-based approaches. As it can be seen, the netlist-based approach always underestimates the overall failure probability. Our analysis reveals that there are two main reasons for this underestimation. First, when there are simultaneous errors at the outputs of the CFI pairs, these transient pulses reach at the same time to the inputs of the fanout gate. In this case, the propagated transients are either completely masked, attenuated, or at least converged to one transient pulse. However, as shown in Figure 1, most of CFI pairs are not physically adjacent in the layout. Second, the forward cones of netlist adjacency pairs are highly overlapped and share similar paths from error sites to the circuit outputs. This can increase the chance that several errors are masked due to one kind of masking (e.g., logical masking in a common gate in the forward cone of both error sites). When MT occurs in error sites which have non-overlapping forward cones, they are independent and the probability of masking is much lower.

On average, netlist-based MT analysis has inaccuracy of 22.34% which is as high as 36.04% for b20 benchmark. Please note that since the information regarding the occurrence probability of different affected gate/flip-flops does not exist at the netlist level, the inaccuracy of those techniques could be even higher.

4.5 Runtime

In order to evaluate the scalability of the proposed layout-based approach to estimate the SER of large circuits, the runtime of layout-based and netlist-based approaches are reported in Table 2. All experiments are done on a workstation with Intel Xeon E5540 2.53GHz and 16GB RAM. As it can be seen, the runtime of layout-based technique is comparable to that of netlist-based technique, i.e., only 15.7% increase in runtime is imposed for layout analysis and extracting MT error sites. The low runtime of the proposed technique is due to the hierarchical layout analysis employed in the proposed approach as detailed in Section 3.1.

5. CONCLUSIONS

In this paper, a fast and accurate layout-based SER estimation technique was presented. Unlike previous techniques

Benchmark	Elements		Runtime [Seconds]		Overhead
	Gates	Flip-flops	Netlist-based	Proposed	
s15850	2,418	513	3.45	3.84	11.3%
s35932	5,328	1,728	11.38	13.28	16.7%
s38417	6,935	1,564	19.23	21.02	9.3%
s38584	7,958	1,275	38.11	47.62	25.0%
b17	17,971	1,317	117.84	132.97	12.8%
b18	54,151	3,020	676.04	782.34	15.7%
b19	99,907	6,042	1836.44	2157.75	17.6%
b20	12,631	430	478.59	562.68	17.6%
Average					**15.7%**

Table 2: Comparison of runtime between netlist- and layout-based approaches

in which the adjacent MT sites are obtained from logic-level netlist, we perform a comprehensive layout analysis to extract MT error sites. It is shown that the layout-based approach is the only viable solution for identification of adjacent cells as netlist-based techniques underestimate the overall SER of the circuit by up to 36.04%. Experimental results show that the layout-based approach has modest runtime and it is scalable for industrial-size circuits.

6. ACKNOWLEDGMENTS

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