Emerging Non-Volatile Memory Technologies for Future Low Power Reconfigurable Systems

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***Abstract*—Non-Volatile Memory (NVM) technologies are promising alternatives to traditional CMOS memory technologies. While NVMs were primarily studied to be used in the memory hierarchy, they can also provide benefits in reconfigurable systems such as *Field-Programmable Gate Arrays* (FPGAs). In this paper, we investigate the applicability of different NVM technologies for the configuration bits of FPGAs and propose a power-efficient reconfigurable architecture based on *Phase Change Memory* (PCM). Quantitative analysis for various FPGA architectures using different memory technologies shows the benefits of the proposed scheme.**

I. Introduction

Emerging *Non-Volatile Memory* (NVM) technologies such as *Spin-Transfer Torque Magnetic Random Access Memory* (STT-MRAM), *Resistive Random Access Memory* (ReRAM), and *Phase Change Memory* (PCM) offer quite higher density, lower leakage power, and more immunity to particle strikes than traditional CMOS memory technologies such as *Static Random Access Memory* (SRAM). The applicability of NVM is not limited to the memory arrays in the on-chip and off-chip memory hierarchy. They can also be exploited in reconfigurable architectures such as *Field-Programmable Gate Arrays* (FPGAs). In addition to the power and reliability advantages of NVMs over the conventional CMOS memory technologies, exploiting NVMs in FPGAs eliminates the need for an additional non-volatile storage such as EEPROM or Flash memory to store configuration bits. This reduces the chip area, removes the boot-up time, and alleviates design complexity at the chip/board level.

Despite appealing features of NVMs, there are several limitations to exploit NVMs in FPGAs such as high write-power consumption and high write-latency during system reconfiguration and high overhead of NVM peripherals. Previously NVM-based FPGA architectures such as [1]–[3] replace conventional SRAM configuration bits as well as user memories such as *Flip-Flops* (FFs) and *Block RAMs* (BRAMs) with NVM cells. However, the power overheads of the specialized *Peripheral Circuitry* (PC) required in NVM-based FPGAs are ignored, which can highly affect the overall power efficiency of the NVM-based FPGAs.

In this paper, we investigate the applicability of various NVM technologies in FPGAs. Based on this study, a power-efficient NVM-based reconfigurable architecture is proposed. To address high power consumption in NVM PCs, the NVM state is converted to the equivalent voltage levels. Quantitative analysis for various FPGA architectures using different memory technologies shows the benefits of the proposed scheme.

II. Applicability of NVMs in FPGAs

In this section we focus on three most mature NVM technologies, namely Flash, STT-MRAM, and PCM. Although PCM and STT-MRAM do not have the maturity of Flash technology, they offer more promising power, performance, and endurance characteristics [4], in addition to lower CMOS integration costs [3]. Moreover, partial reconfiguration is not fully supported in Flash-based FPGAs due to block erasure limitation of Flash technology. PCM and STT-MRAM are both resistive memories and represent the stored data by corresponding resistance values. As a result, a PC is required to convert the cell resistance to the equivalent voltage level. In regular array memory structures such as cache and main memory, the PC usually employs a sense amplifier which could be shared by multiple cells, e.g. the entire column. In contrary, configuration bits in FPGAs are structured in a large number of small frames. Although, it is possible to share the traditional NVM PCs for the configuration bits of a frame, with the large number of frames, the overhead of PCs will be still significant. Additionally, a continuous read from all configuration bits is required after FPGA power-up. Therefore, the PC overhead could not be shared among multiple cells in FPGAs and each configuration frame requires a dedicated PC. Consequently, using a PC structure per configuration frame, same as those used in regular array memory structures, could impose significant energy and area overheads in FPGAs.

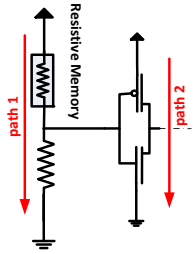

Fig. 1. Resistive memory PC model

All previously proposed PCs for PCM- and STT-MRAM-based FPGAs can be modeled by a simple voltage divider circuit as demonstrated in Fig. 1. While the ratio of high to low resistance states (R_H/R_L) in STT-MRAM is less than 4 [7], this is as high as 10^4 in PCMs [8]. This eliminates the need for an inverter or a buffer at the output of the voltage divider and as a result, reduces the short-circuit power through path 2 (Fig. 1). Furthermore, PCM offers higher R_H compared to STT-MRAM which could further reduce the leakage current in path 1 (Fig. 1). Table I shows the static power of STT-MRAM based PC proposed in [6] as compared to a single

TABLE I. Static Power Consumption and Simulation Parameters

Circuit	Static Power (Watt)			Simulation Parameters
	Path 1	Path 2	Total	
Inverter	-	-	1.0E-08	W/L: 3/2, Vss:1V, $45nm$
SRAM	-	-	7.2E-08	W/L: same as [5], Vss:1V, $45nm$
PC [6]	5.6E-05	2.1E-06	5.8E-05	R_H:$6K\Omega$, R_L:$2K\Omega$, Vss:1V

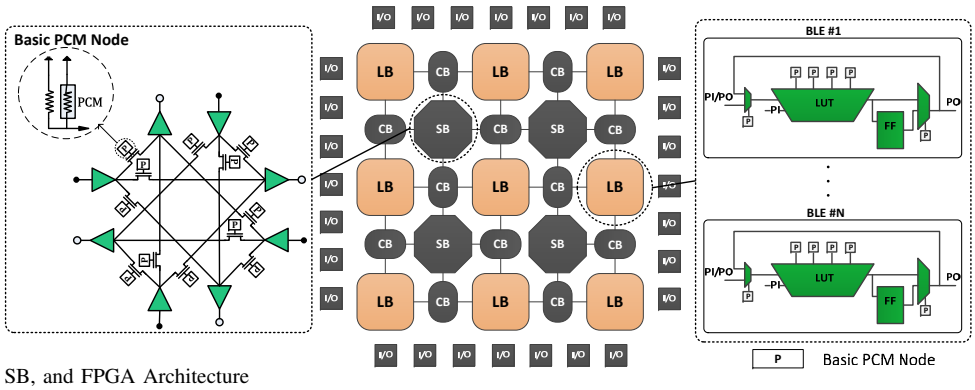

Fig. 2. Proposed LB, SB, and FPGA Architecture

SRAM cell and an inverter. The static power consumptions through path 1 and path 2 are orders of magnitude more than the total static power consumption of a single SRAM cell. As a result, PCM cells are exploited in our proposed power-efficient reconfigurable architecture.

III. Proposed Architecture & Results

Fig. 2 demonstrates an overview of the proposed PCM-based FPGA architecture. Same as the conventional *SRAM-based FPGAs* (SFPGAs), the proposed architecture consists of an array of *Logic Blocks* (LBs) that are connected to each other through programmable *Switch Boxes* (SBs) and *Connection Blocks* (CBs). In the proposed SB and *Look-Up Table* (LUT) structures, which are similar to those in the conventional SFPGAs, the SRAM cells are replaced with the basic PCM node presented in Fig. 2. Despite static leakage current in each basic PCM node, the simulation results demonstrate that the overall leakage power is less than that of the SRAM-based structures. The proposed basic PCM node consists of a resistor connected to a PCM cell. This PCM node is, in fact, a simple voltage divider circuit. This circuit is used to convert the PCM state to the equivalent voltage level. The resistor value is opted to reduce the leakage current and also to provide the appropriate voltage level at the output. Since the PCM technology offers high R_H/R_L values, there is no further need for a buffer or inverter at the output of the voltage divider. This further reduces the static power by avoiding the short-circuit leakage in the buffer/inverter.

In order to evaluate the proposed PCM-based FPGA, we compare our proposed architecture with the conventional SRAM-based FPGA and the PCM-based FPGA proposed by Gaillardon et. al. [3]. In the experiments, Cluster size (N) of 4 and LUT size (K) of 6 is used for all of the architectures. VPR 6.0 is used to cluster, place, and route 20 largest MCNC benchmark circuits. Then the power, performance, and *Power Delay Product* (PDP) results are extracted by Hspice simulations.

The proposed architecture can improve power and PDP up to 37.7% and 35.7%, respectively with negligible (3.2%) performance overhead as compared to the SFPGAs. The negligible difference is caused by different performance characteristics between the proposed basic PCM node and an SRAM cell.

The proposed architecture reduces the total power consumption by 15.2%, 22.2%, and 37.7% in 130, 90, and 45nm technologies, respectively, as compared to the SRAM-based FPGA. This means that the benefit of the proposed architecture is pronounced with technology scaling. In addition, the total power consumption is reduced in the proposed architecture by 77.0%, 77.3%, and 76.8% in 130, 90, and 45nm technologies, respectively, as compared to the proposed FPGA by Gaillardon. This means that using PCM technology by itself does not guarantee the power efficiency and even can impose significant power consumption overheads. This reveals the important role of power efficiency of PCs in NVM-based FPGAs. Furthermore, the results indicate the potential of the proposed architecture to reduce the power consumption as the technology size decreases.

IV. Conclusion

In this paper, we investigated the applicability of various NVM technologies in FPGA configuration bits. Based on this analysis, we proposed a PCM-based FPGA architecture by developing a power-efficient peripheral circuitry for SBs and LUTs. The results showed that the proposed architecture can improve power consumption and PDP up to 37.7% and 35.7%, respectively, with minimal performance overhead.

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