Layout-Based Modeling and Mitigation of Multiple Event Transients

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***Abstract*—Radiation-induced multiple event transients (METs) are expected to become more frequent than single event transients (SETs) at nanoscale CMOS technology nodes. In this paper, a fast and accurate layout-based soft error rate (SER) assessment technique with consideration of both SET and MET fault models is presented. Despite existing techniques in which the adjacent MET sites are extracted from a logic-level netlist, we conduct a comprehensive layout analysis to obtain MET adjacent cells. Experimental results reveal that the layout-based technique is the only viable solution for identification of the adjacent cells as netlist-based techniques considerably underestimate the overall SER. Furthermore, by identifying the most vulnerable adjacent cells and increasing their physical distance in the layout using local adjustment rules, we are able to considerably reduce the overall SER without imposing any area and performance penalty.**

***Index Terms*—Multiple bit upset (MBU), multiple event transient (MET), reliability, soft errors.**

I. Introduction

DOWNSCALING of transistor feature size and operating voltage coupled with ever increasing device count per chip (i.e., Moore's law) result in a significant increase in the susceptibility of circuits to soft errors over the past years [1], [2]. In the absence of protection techniques, the system soft error rate (SER) grows in direct proportion to the number of cells in the design [2], [3]. Although there has been extensive efforts on the research and development of radiation-hard spintronic-based technologies [4]–[6], they are not included in the current design flow. Hence, identification of the most vulnerable components using a fast and accurate SER estimation technique and applying low-cost selective protection schemes is of decisive importance.

Transient errors caused by a single particle strike in sequential elements (i.e., memory cells, latches, and flip-flops) and combinational gates are called single event upset (SEU) and single event transient (SET), respectively. SEU and SET fault models have been extensively studied over the recent years [7]–[10]. With miniaturization of device geometries in nanoscale technologies, it is very likely that a high energy particle strike affects several adjacent cells in a circuit resulting in multiple bit upsets (MBUs) in sequential elements [11]–[14] or multiple event transients (METs)[1] in combinational gates [15].

In the previous technology nodes, soft errors had a considerable effect only in sequential elements which were significantly mitigated by means of error correcting codes [16]–[19] and built-in soft error tolerance schemes [20]–[23]. Recent experiments reveal that the contribution of combinational gates is also considerable in nanoscale technologies [24]–[26]. Furthermore, it is claimed that a remarkable fraction of particle strikes results in MET [15], [27]. In order to cost-effectively mitigate both SETs and METs, their impacts at the layout and logic levels must be accurately modeled.

The analytical techniques presented in [28] and [29] address the MET fault model in logic circuits. The error probability propagation-based technique presented in [28] propagates the error probabilities from the error sites toward both primary outputs and sequential elements. The technique presented in [29] is based on Boolean decision diagrams and provides more accuracy at the expense of runtime, compared to the earlier method. The major shortcoming of these techniques in estimating SER due to METs is that they use logic-level netlist for identification of MET error sites, neglecting layout-level adjacency of error sites. Such assumption can significantly underestimate the circuit SER as we will experimentally demonstrate later in this paper. Additionally, the distribution of affected error sites and the number of affected cells completely depends on the layout-level details and cannot be extracted from the logic-level netlist. For example, our experiments show that a considerable fraction of particles simultaneously affects both combinational gates and flip-flops, which is completely ignored in previous techniques. Ignoring such cases can further increase the SER inaccuracy. In the rest of this paper, the occurrence of multiple transient (MT) errors at sequential elements, combinational gates, or combination of them is called MT.

The MT rate could be considerably affected by the placement strategy [30], hence, several placement techniques [31]–[33] has been proposed to adjust the spacing among cells according to the pulse quenching mechanism.

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[1]Also known as single event multiple transient.

Pulse quenching is caused by the charge sharing phenomenon and could affect the generated pulse width [34]. Such placement techniques ignore the logical and electrical masking which could occur in any of the common gates in the forward cones of the affected cells. Therefore, a more generic placement strategy is required to exploit the entire MT mitigation potential to reduce the failure probability.

In this paper, we provide analysis and mitigation for the effect of MTs at the layout-level. We first present a fast and accurate technique for SER estimation considering the effect of MTs at the circuit layout. In the proposed technique, the surface affected by a particle in combinational and sequential logic is estimated with oval shapes obtained from available MBU patterns[2] in memory arrays. Considering MBU patterns occurrence probability, ovals are randomly placed at different locations inside the circuit and the list of affected cells is extracted. Then, logic level analysis with multiple error propagation is performed to obtain the overall SER. Furthermore, we investigate the impact of technology scaling on MTs and the failure probability. Analysis of ISCAS'89 and ITC'99 benchmark circuits reveal that only less than 10% of the netlist adjacent cells are physically adjacent in the layout. Also, more than 60% of physically adjacent cells are not adjacent in the netlist. Experimental results show that neglecting layout adjacency can cause inaccuracy up to 36.04% in the circuit overall SER.

In addition, by performing a detailed analysis on the results of MT modeling, we identify several MT mitigation opportunities which can be applied during the placement. These opportunities are exploited to locally adjust the position of cells in the layout based on the vulnerability of MT affecting adjacent cells. The experimental results show that this technique is able to considerably reduce the overall SER of the employed benchmark circuits without any area and performance penalty. This technique is built on top of an existing commercial place & rout tool and has a modest runtime and is scalable for industrial size circuits.

A preliminary version of this paper was published in [35] which focused on the MT modeling. In this paper, we extend the MT modeling by investigating the impact of technology scaling on MTs. This is done by applying the proposed MT modeling for a 45 and 15 nm standard cell libraries. Additionally, we also introduce several opportunities for MT mitigation during physical design and exploit them to propose a scalable MT mitigation technique during the physical design process. This technique could efficiently reduce MTs without imposing any area and performance overhead.

The remainder of this paper is organized as follows. Section II motivates the layout-based MT modeling and investigates the validity of the netlist-based adjacency assumption used in previous techniques. In Section III, the proposed layout-based approach is explained followed by its experimental results in Section IV. The proposed MT-aware placement and related experimental results are presented in Sections V and VI, respectively. Finally, the conclusion is given in Section VII.

[2]The spread of the affected cells due to a single particle strike in SRAM array is called MBU pattern.

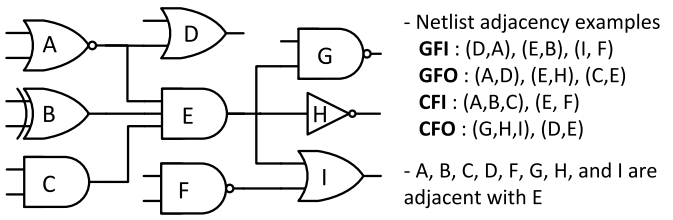

Fig. 1. Examples of different adjacency scenarios considered in the netlist.

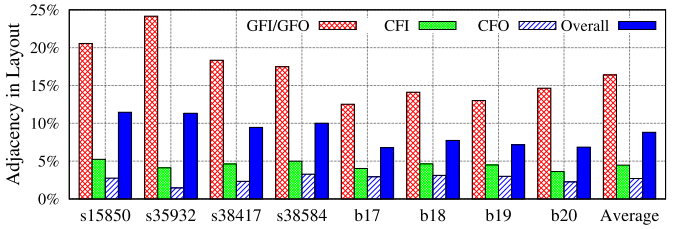

Fig. 2. Relevance of different adjacency scenarios considered in the netlist to layout adjacency.

II. Motivation for Layout-Based MT Analysis and Mitigation

An important step in MT analysis is identifying physically adjacent cells as error sites. Although the layout of the circuit is necessary for the accurate identification of adjacent cells, the previous MT analysis techniques presented in [28] and [29] employ some heuristic approaches to extract the list of adjacent cells from the netlist. In these techniques, four categories including a gate and its fan-in (GFI), a gate and its fan-out (GFO), common fan-ins of a gate (CFI), and common fan-out of a gate (CFO) are considered as adjacent nodes for MT error sites. Fig. 1 shows several examples of netlist-based adjacencies. In these techniques, a gate is first selected as primary error site and then its MT pair are randomly selected among its netlist adjacent cells.

In order to check the accuracy and layout-relevance of this model, i.e., extraction of adjacent cells from the logic netlist, the layout of several circuits selected from ISCAS'89 [36] and ITC'99 [37] benchmarks synthesized with respect to Nangate 45 nm have been comprehensively analyzed (the details of this analysis framework is provided in Section IV). In this regard, all possible adjacent pairs for different netlist adjacency categories are first extracted from the netlist and then the physical adjacency of each pair in the circuit layout is investigated. Since the order of adjacent pairs is not important in this investigation, both GFI and GFO categories are equal and are assumed as a single category called GFI/GFO. In the example given in Fig. 1, E is the fanout of gate B and gate B is a fan-in of gate E. As a result, pair (B, E) belongs to both GFI and GFO categories. Fig. 2 shows the results of this experiment. As it can be seen, on average, only less than 10% of netlist adjacent pairs are also adjacent in the circuit layout.

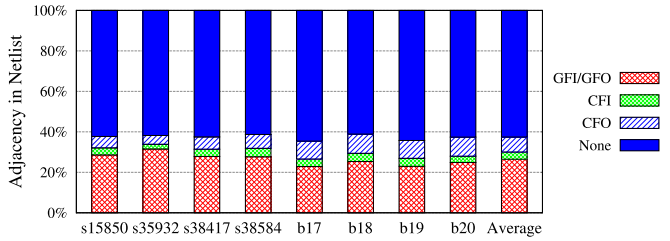

Fig. 3. Relevance of extracted adjacencies from layout to netlist-level MT error models.

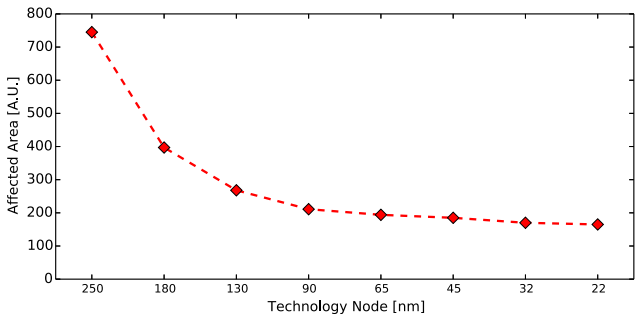

Fig. 4. Average affected area for neutron particles across different technology nodes based on the cell and MBU size information reported in [2].

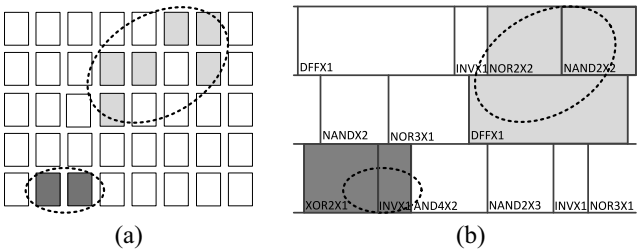

Fig. 5. Extraction of MT error sites from existing MBU patterns. (a) Two MBU patterns in SRAM. (b) Equivalent MT error sites in circuit layout.

Also, the probability of physical adjacency of GFI/GFO category is much higher than that of CFI and CFO categories.

There is another experiment conducted in which all layout adjacencies on the circuit layout are first extracted and then for each physical adjacency, its netlist adjacency category is investigated (Fig. 3). It can be inferred from Fig. 3 that more than 60% of the physical adjacencies do not belong to the previously defined netlist adjacency categories.

From these two experiments, it is clear that there is no statistically meaningful correlation between netlist and layout adjacencies. This means that for an accurate MT analysis, netlist-level analysis for MT error site abstraction is not sufficient and layout-level analysis must be performed. To address this issue, we propose a fast and accurate layout-based MT modeling technique. This technique can also guide MT-aware physical design to mitigate MTs as netlist-based MT mitigation cannot be effective due to the inaccuracy of netlist-based MT analysis.

III. Proposed Layout-Based MT Modeling

In this section, the proposed layout-based SER estimation approach with consideration of MT fault model is explained. This approach has two main steps, layout-based MT error site extraction and multiple error propagation at logic-level.

A. Layout-Based MT Error Site Extraction

1) MT Error Site Extraction Using MBU Analysis: The first step for accurate MT modeling is extracting physically adjacent error sites from the circuit layout. This requires to have MT patterns projected in the circuit layout and their occurrence probabilities. To the best of our knowledge, no field results about MT patterns on combinational and sequential logic have been reported in the literature. This could be mainly due to the fact that the logic gates and sequential elements (such as flip-flops) have significantly less observability as compared to regular structures such as SRAM-based memory arrays. Since memory arrays are more regular and dense than logic structures and also have a full observability, the affected area can be accurately estimated.

In this paper, we try to use available MBU patterns in memory arrays for identification of MT error sites in logic circuits. In this method, it is assumed that the surface affected by a particle strike is almost the same for the memory arrays and logic cells in different technology nodes. In order to support this assumption, the average affected area of SRAM for neutron-induced particle strikes across different technology nodes are reported in Fig. 4. These results are extracted according to the cell area and MBU size information reported in [2]. Basically SRAM cells act as a guideline for determining the affected area and smaller cell size could provide more accurate results due to high resolution in estimating the area. As it can be seen from this figure, the estimated affected area reduces from 250 to 90 nm which is mainly due to larger SRAM cell size, and hence, less resolution in the area estimation. However, the estimated affected area is relatively constant from 90 to 22 nm, independent of the cell size. This clearly shows that the affected area is independent of the underlaying SRAM technology. Hence, it could be conclude that the affected area would be also the same for the irregular logic circuits.

The main idea behind this paper is to extract the affected area in a memory array and then consider all logic cells covered by a similar surface to be MT error sites. In this regard, the affected area for each MBU pattern is first extracted. Predominant MBU patterns in memory arrays have been comprehensively studied using neutron beam-based accelerated SER estimation [11], [12], [38]. The number of affected bits by a single strike depends on several parameters including particle type and its energy, strike angle, cell type, cell size, and output load [13]. Given memory cell dimension as well as vertical and horizontal distance between adjacent cells, for each MBU pattern the surface affected by the strike can be calculated. Most of the MBU patterns, especially MBUs with more than eight bits, can be effectively covered by an oval surface. As a result, in our approach as shown in Fig. 5, all cells affected by an MBU are first surrounded by an oval. Then, during SER estimation the same oval is transferred to random locations inside the logic layout and all cells affected by the MT are listed as error sites.

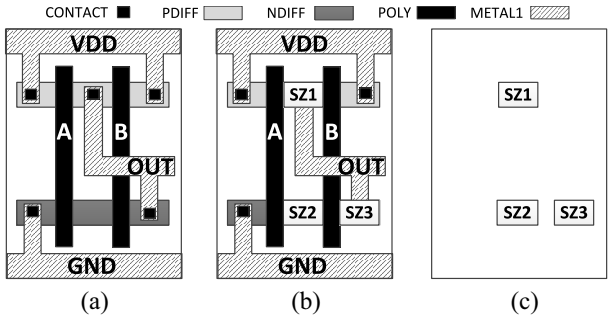

Fig. 6. Sensitive zone (SZ) extraction for a NAND gate. (a) Cell layout. (b) Identification of diffusion parts which are not connected to supply voltage. (c) Sensitive zones (adapted from [39]).

Algorithm 1: Layout-Based SER Estimation

1 Extract a surrounding oval for each MBU pattern
2 Extract sensitive zones of each cell by library characterization
3 Divide layout into smaller grids and extract the list of cells in each grid
4 **while** *sampling error < predefined value AND number of cells covered by at least one MT < 99.9%* **do**
5 Randomly select an oval based on their occurrence probability
6 Place the oval in a random location on the layout
7 Find the list of grids which have overlap with the oval
8 Search overlapped grids cell lists and construct overlapped cells list
9 Remove cells without overlapped sensitive zones from cell list
10 Mark all cells in overlapped cell list as covered by an MT
11 Propagate MT at logic-level and calculate failure probability
12 **end**
13 Report average failure probability

2) Library Characterization: In the circuit layout, only a subset of cells which have an overlap with the oval surface are considered as error sites. A cell has overlap with an oval surface if at least one of the sensitive zones to soft errors (*N*-diffusion and *P*-diffusion) falls within the surface. In fact, when a particle strikes a cell, it causes an additional charge to be collected in the diffusion parts of the transistor which in turn disturbs the normal operation of the transistor. The charge collected to the diffusion parts which are connected to VDD and GND pins is evacuated and does not affect the circuit behavior. The other parts of the diffusion can be disturbed by collection of additional charge. Fig. 6 shows how sensitive zones for a NAND gate layout are extracted based on this explanation. Using this approach, all cells inside the technology library are characterized and sensitive zones coordinations are extracted.

3) Overall Flow: The main steps of the proposed layout-based SER estimation are summarized in Algorithm 1. Initially, the list of ovals and their occurrence probability are extracted from existing MBU patterns (line 1) and then technology library is characterized for identification of sensitive zones (line 2). These two steps are performed once in advance and their results are used for all circuits to be analyzed in the same technology and library settings.

Due to the large number of cells and sensitive zones inside industrial-size circuits, a hierarchical approach is employed to minimize the time needed for identification of error sites affected by an MT (line 3). In this approach, the entire layout area is divided into smaller grids and the list of cells inside each grid is extracted. During SER estimation, instead of searching among large number of cells, in the first step, for each grid it is checked whether it has an overlap with the oval surface and the list of layout grids overlapped by the oval surface is extracted. Then, the list of overlapped cells is extracted by investigation of cells inside overlapped layout grids. At the end, those cells which have no overlapping sensitive zone with the oval surface are eliminated from the target cell list. The remaining cells will be used as candidate MT fault sites (lines 7–9).

B. Multiple Error Propagation

In the layout-based MT error sites extraction, it is quite possible that flips-flops and combinational gates are simultaneously affected by an MT. This issue is completely ignored in the previous work. In such scenarios, a transient pulse is produced at the output of affected cells while the value stored in flip-flops are logically inverted. To handle such cases, a fast and accurate propagation mechanism is required.

During multiple error propagation, unified treatment of three timing masking factors, i.e., logical, electrical, and latching-window, is essential for accurate SER estimation [40], [41]. The four-value logic (0, 1, 0^e, 1^e) [28] which offers an effective tradeoff between runtime and accuracy, is employed to compute the logical masking factor. This technique can efficiently handle the effect of single error propagation in reconvergent paths as well as the effect of multiple errors propagation in convergent paths. For electrical masking factor, the equation-based transfer function presented in [42] is adopted. This technique models a transient pulse using a trapezoidal model and can accurately compute the electrical attenuation. Latching-window masking model is based on the well-known and widely used equation presented in [43].

It is quite possible that an MT does not propagate to the primary outputs in the first cycle, but it may be latched in some flip-flops and propagates to the primary outputs in the subsequent cycles. Experimental results in [44] reveal that failure probability saturates in few cycles (normally less than ten cycles) after error occurrence. Therefore, multicycle error propagation is also taken into account in our framework.

While propagating errors along combinational gates, all three masking factors should be considered in the first cycle. At the end of the first cycle, the error is either captured in the flip-flops or eliminated (masked) from the system. In the subsequent cycles, only logical masking factor can prevent the error from propagation and as a result, the other masking factors are ignored. In contrast, when a strike affects a flip-flop, in all cycles including the first cycle, only logical masking is taken into account. In case of simultaneous error occurrence at both logic gates and flip-flops, all three masking factors have been considered in the first cycle. However, the width of the output transient pulse of erroneous flip-flops is set to be equal to the clock period to overcome the latching-window masking factor for such errors.

C. Combined Layout and Logic SER Analysis

Since there are many oval shapes and each oval can be placed in different locations of the circuit layout, there are

infinite MT scenarios even for very small circuits. Therefore, we use a Monte Carlo simulation-based approach to extract the overall SER of the circuit with respect to MT. In this approach, in each iteration, based on the MBU patterns occurrence probability, one of them is randomly selected and its corresponding oval will be placed in a random location on the layout. After extracting the list of affected cells using the hierarchical approach, the errors are propagated from the error site and the failure probability for this MT is calculated. This continues until reaching a predefined accuracy level. An equation to compute the sampling error of Monte Carlo simulations with respect to the number of iterations and the obtained failure probability is provided in [45]. The MT analysis terminates when the sampling error is less than the predefined value and the number of cells contributed in the MC simulations by at least one MT exceeds 99.9%. The second condition is used to make sure that most of the cells in the layout has been considered during SER estimation.

IV. Experimental Results of MT Modeling

Using the proposed layout-based MT error site extraction and combined combinational and sequential multiple error propagation at logic-level, we have performed an extensive analysis on the impact of particle energy on the MT error sites. By performing experiments on both Nangate 45 nm (planner) and 15 nm (FinFET) technology nodes, we were able to show the impact of technology scaling on MT size. Additionally, the impact of netlist adjacency assumption on the overall SER of the circuit is investigated.

A. Work Flow

In order to show the scalability of the proposed approach, we have evaluated the largest available benchmark circuits in ISCAS'89 and ITC'99 benchmarks suites. For each benchmark, the HDL description of the circuit is first synthesized using a Synopsys Design Compiler [46] for the maximum possible operational clock frequency.[3] Then, the layout of the netlist is extracted using Cadence SoC Encounter [47] by considering utilization ratio of 75% (typically about 65%–85% [48]). The minimum clock period as well as the chip area for each circuit are reported in Table I. According to these results, the area and frequency are decreased by around $4\times$ for the circuit synthesized for 15 nm compared to 45 nm.

The MBU patterns for particles with 22, 37, 95, and 144 MeV provided by [11] are used during the layout-based MT extraction. This information is given to our layout-based SER estimation to calculate the overall SER of the circuit according to Algorithm 1. In our framework, SER estimation analysis terminates when the maximum inaccuracy of the Monte Carlo is less than 0.5%. In this experiment, the layout is divided into 30×30 μm^2 grids, where each grid includes around 800 cells.

[3]This requires two rounds of synthesis. The first round is for obtaining the maximum operational frequency. In this round, the clock period is set to zero to force the synthesis tool to implement all paths as short as possible. The maximum negative slack obtained shows the maximum operational frequency. Then, another synthesis operation is performed in the second round to minimize the area and power for the maximum operation frequency.

TABLE I
Minimum Clock Period and Area of Benchmark Circuits Synthesized Into 45 and 15 nm Nangate Standard Cell Libraries

Benchmark	Nangate 45 nm		Nangate 15 nm	
	Clock Period [ps]	Area [μm^2]	Clock Period [ps]	Area [μm^2]
s15850	825	9,134	184	2,723
s35932	487	32,735	105	9,669
s38417	924	27,760	139	9,320
s38584	610	28,709	121	8,754
b17	1,357	32,175	331	8,451
b18	2,133	101,200	549	27,200
b19	2,046	194,360	530	52,232
b20	1,734	29,433	452	8,259

TABLE II
Average Area Affected With Different Particle Energies

Particle Energy (Mev)	Average Affected Area (μm^2)
22	1.178
47	1.902
95	2.903
144	4.613

The failure probability in this paper is defined according to [44] as the probability of propagation from error sites to primary outputs during first few cycles after error occurrence. The error is propagated for ten cycles and all three masking factors have been considered during error propagation.

B. MBU Patterns and MT Error Sites

As mentioned earlier, in order to extract MT error sites, the area affected by MBU patterns are first extracted and then a surrendering oval for each MBU pattern is constructed. These ovals are used for identification of MT error sites. For this purpose, detailed information about different MBU patterns in a memory array is necessary for identification of MT error sites.

Radaelli *et al.* [11] have reported detailed information about predominant MBU patterns in a 150 nm technology SRAM device and their occurrence probability for particles with 22, 47, 95, and 144 MeV energies. Considering the SRAM cell dimensions, the area affected by each MBU surrounding oval can be accurately estimated. For these cases, the oval shapes and their occurrence probability (same as the occurrence probability of the corresponding MBU pattern) are computed. Table II shows the average area affected by each particle energy obtained by wighted averaging of oval surfaces based on their occurrence probability.

The area affected by a particle strike is mostly a function of particle energy, while the strength of the transient pulse mostly depends on other parameters such as diffusion volume (width, length, depth) and load capacitance [2]. As a result, the affected area information acquired for a 150 nm SRAM technology can also be used for the logic area affected by a particle strike with the same energy in the 45 and 15 nm technology nodes. Please note that although the affected area remains constant, however, due to the technology downscaling, the number of affected cells increases in smaller technologies.

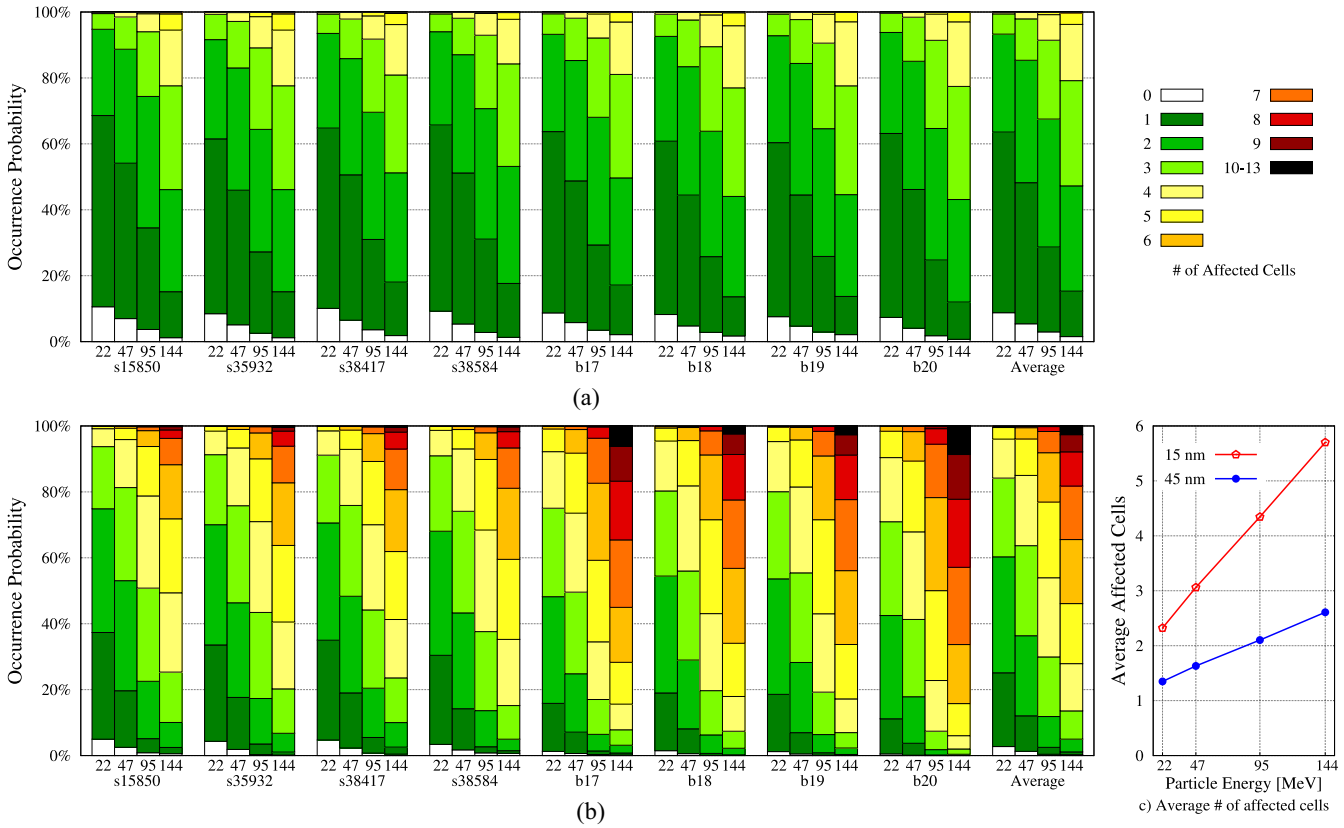

Fig. 7. Distribution of # of cells (flip-flops or combinational gates) affected by particle strikes with 22, 47, 95, and 144 MeV energies for benchmark circuits synthesized with respect to (a) 45 nm and (b) 15 nm Nangate standard cell library as well as (c) average affected cells per technology node.

By randomly locating these ovals on the circuit layout according to their occurrence probability, different combinations of affected combinational gates and flip-flops are extracted and identified as MT error sites. Fig. 7 shows the occurrence probability of different number of affected cells for particle strikes with 22, 47, 95, and 144 MeV energies. As it is expected, by increasing the particle strike energy, the occurrence probabilities of SET and SEU decreases significantly and MT becomes predominant. In addition, the MT ratio in 15 nm is significantly larger than that in 45 nm.

In this experiment, the maximum number of affected cells at 45 and 15 nm are 8 and 13 cells, respectively. In order to clearly show the impact of technology scaling on MT rate, the average number of affected cells for the aforementioned particle energies are reported in Fig. 7(c). This figure reveals that the average number of affected cells is almost doubled for all particle energies from 45 to 15 nm. Hence, accurate modeling and mitigation of MTs are more challenging in smaller technology nodes with larger number of affected cells.

In previous netlist-based techniques [28], [29], it is assumed that a particle strike leads to either MET on combinational logic or MBU on sequential cells. Also, the number and type of affected cells was a function of the particle energy rather than a function of the layout. However, our results show that: 1) adjacent combinational and sequential cells can be simultaneously affected by a single particle strike and 2) the number, type, and the combination of affected cells depend on the layout structure as well.

C. Error Generation

Although the affected area information could be acquired from MBU patterns, the pulse width of generated SETs is completely technology dependent [49], [50]. In order to obtain the distribution of the generated pulse widths in each technology node for a certain particle energy, we exploit a commercial tool [51]. The functionality of this tool was verified using radiation testing results. This tool first characterizes the standard cells using a set of TCAD simulations to generate a process response model. Using this process response model and by taking into account the physical layout of the standard cell, the sensitivity of the cell is obtained by injecting a set of current pulses in the SPICE netlist of the cell. This tool extracts the list of transistors subject to the charge sharing effect [52] from the cell layout and models it by adding multiple current sources to the SPICE netlist.

In this paper, for a given particle energy, the distribution of pulse widths for each standard cell was generated using this tool. For error generation, we exploited such distributions to generate random pulse widths in the affected combinational gates. Several representative examples of pulse width distribution for Nangate 45 nm and more details about the error generation step could be found in [26].

D. Impact of SET/SEU Versus MT Model on Overall SER

In order to explore the importance of MTs and technology scaling impact on the failure probabilities, overall SERs

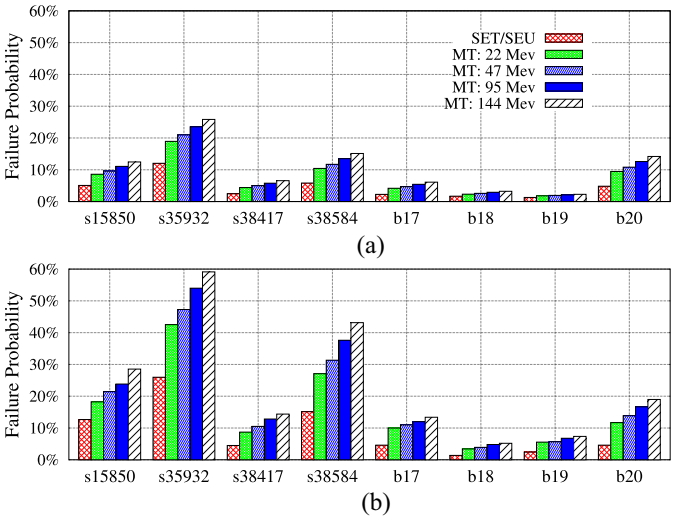

Fig. 8. Average failure probabilities of different particle energies for circuits synthesized with respect to Nangate (a) 45 nm and (b) 15 nm standard cell.

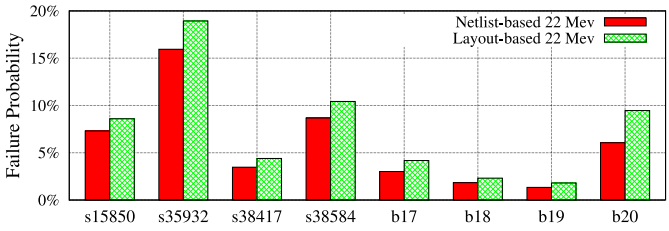

Fig. 9. Comparison of overall SER obtained by netlist-based and layout-based approaches for circuits synthesized for Nangate 45 nm standard cell library and particle with 22 MeV energy.

extracted for particles with 22, 47, 95, and 144 MeV energies are compared with the case that the simple SET/SEU model is considered for both 45 and 15 nm technology nodes (Fig. 8). In case of SET/SEU, a single error is injected in each gate/flip-flop and the average of the failure probabilities of all cells are reported as the circuit failure probability. All MT error sites are extracted from layout and propagated using the propagation method explained in Section III-B.

The results shown in Fig. 8 reveal that the average failure probability significantly increases from 45 to 15 nm (by more than 2× in some cases). One reason for such an increase is that the number of affected cells is almost twice in the smaller technology node [as shown in Fig. 7(c)]. Another interesting reason is higher operational frequency and smaller latching window of the circuits designed with Nangate 15 nm (see Table I) which significantly affects the error latching probability. The average latching windows of flip-flops in 45 and 15 nm are 42.4 and 12.7 ps, respectively. As shown in [53], the combinational logic SER linearly grows by increasing the frequency due to increased ratio of latching window to the entire clock period.

The results also reveal that the circuit failure probability does not linearly increase with the particle energy. As an example, on average, the SER in the presence of 47 MeV particles is only 1.15× greater than when considering 22 MeV particles. This can be explained by the number of affected cells for different particle energies as reported in Fig. 7.

It worth to mention that, in this paper, we only report the failure probability for four specific particle energies. As mentioned earlier, the failure probability metric only shows the error propagation probability for a generated error, however, the particle strike rate has to be also taken into account for computing SER. In fact, SER is computed as multiplication of particle strike rate and failure probability by considering the entire energy spectrum. Computing SER of a circuit requires a very detailed information about struck rate of particles with different energies in the environment under study and their corresponding MBU patterns. Since such information is technology dependent and requires detailed radiation characterization of that technology, in this paper, we only focus on the failure probability of several representative particle energies.

One reasonable solution to show the SER trend from 45 to 15 nm is to investigate the tradeoff between failure probability increase and the decrease in the particle strike rate across different technology nodes. As shown in Table I, the area and clock period of circuits in 15 nm are reduced by 3.5× and 4.6× compared to 45 nm. This means 15.8× less particles strikes for a certain task running on a circuit fabricated in 15 nm due to the smaller area and shorter runtime. On the other hand, the failure probability grows on average by 2.2× from 45 to 15 nm (see Fig. 8). Hence, the overall trend would be 7.2× reduction in the overall SER. These results are inline with that of [50], [54], and [55].

E. Impact of Netlist Adjacency Assumption on SER

In order to investigate the effect of netlist adjacency on the overall SER, we have implemented a netlist-based approach. The error propagation method of the netlist-based approach is similar to the one explained in Section III-B. Although different combinations of affected cells and their occurrence probability are unknown at the netlist-level, in order to have a fair comparison, the same occurrence probabilities is also used in the netlist-based approach. Fig. 9 reports the failure probability obtained by both netlist- and layout-based approaches. As it can be seen, the netlist-based approach always underestimates the overall failure probability. Our analysis reveals that there are two main reasons for this underestimation. First, when there are simultaneous errors at the outputs of the CFI pairs, these transient pulses reach at the same time to the inputs of the fanout gate. In this case, the propagated transients are either completely masked, attenuated, or at least converged to one transient pulse. However, as shown in Fig. 1, most of CFI pairs are not physically adjacent in the layout. Second, the forward cones of netlist adjacent pairs are highly overlapped and share similar paths from error sites to the circuit outputs. This can increase the chance that several errors are masked due to one kind of masking (e.g., logical masking in a common gate in the forward cone of both error sites). When MT occurs in error sites which have nonoverlapping forward cones, they are independent and the probability of masking is much lower.

On average, netlist-based MT analysis has an inaccuracy of 22.34% which is as high as 36.04% for b20 benchmark.

TABLE III
COMPARISON OF RUNTIME BETWEEN NETLIST- AND LAYOUT-BASED APPROACHES

Benchmark	# of Elements		Runtime [Seconds]		Overhead
	Gates	Flip-flops	Netlist-based	Proposed	
s15850	2,418	513	3.45	3.84	11.3%
s35932	5,328	1,728	11.38	13.28	16.7%
s38417	6,935	1,564	19.23	21.02	9.3%
s38584	7,958	1,275	38.11	47.62	25.0%
b17	17,971	1,317	117.84	132.97	12.8%
b18	54,151	3,020	676.04	782.34	15.7%
b19	99,907	6,042	1836.44	2157.75	17.6%
b20	12,631	430	478.59	562.68	17.6%
Average					**15.5%**

Please note that since the information regarding the occurrence probability of different affected gate/flip-flops does not exist at the netlist level, the inaccuracy of those techniques could be even higher.

F. Runtime

In order to evaluate the scalability of the proposed layout-based approach to estimate the SER of large circuits, the runtime of layout-based and netlist-based approaches are reported in Table III. All experiments are done on a workstation with Intel Xeon E5540 2.53 GHz and 16 GB RAM. As it can be seen, the runtime of layout-based technique is comparable to that of netlist-based technique, i.e., only 15.7% increase in runtime is imposed for layout analysis and extracting MT error sites. The low runtime of the proposed technique is due to the hierarchical layout analysis employed in the proposed approach as detailed in Section III-A.

V. MT-AWARE PLACEMENT

As shown in Fig. 7 and confirmed by [14], [15], and [27], it is highly probable that one strike affects multiple adjacent cells in the layout. The experimental results in [30] show that the placement strategy could significantly affect the SER of a circuit. Thus, one can employ various optimizations of cell placement to significantly alleviate the effect of MTs. To this end, we propose a generic approach to identify the most vulnerable pairs of cells and subsequently increase their physical distance in the layout.

A. Opportunities for MT-Aware Placement Optimization

The proposed MT-aware placement is based on the following optimization opportunities.

1) *Non-Uniform Cell Density:* Since the routing is the limiting factor in irregular structures (i.e., random logic) fabricated with nanoscale technology nodes [56], there are always some whitespace (i.e., unused space) among cells in the layout. Hence, the layout utilization ratio[4] is typically between 65%–85% [48]. Existing commercial place & route tools (e.g., Cadence SoC Encounter) uniformly place the cells across the die, however, the sensitivities of the cells to soft errors are quite nonuniform. The nonuniformity of MT failure probability on the physical layout of b18 and b19 benchmark circuits are depicted in Fig. 10. This is obtained by injecting one million errors at random locations of the layout (similar to our experiments in Section IV). Since nodes with very small failure probabilities have much less contribution to the overall SER, it makes sense to reduce the spacing between less vulnerable cells and exploit this space to increase the spacing among highly vulnerable cells. In other words, the cell spacing should be nonuniform and proportional to the MT soft error vulnerability.
2) *Error Masking Potential of MTs:* Our experimental results in Section IV-E showed that failure probability obtained based on the netlist-based adjacency assumption is on average 22.34% less than that estimated by the layout-based approach. The main reason for the smaller failure probability of the netlist-based approach is that the errors propagated from adjacent cells have chance to interact and cancel out each other (i.e., getting masked). For example, in the gate-level netlist shown in Fig. 11(a),

[4]The ratio of overall area occupied by cells to the entire chip area.

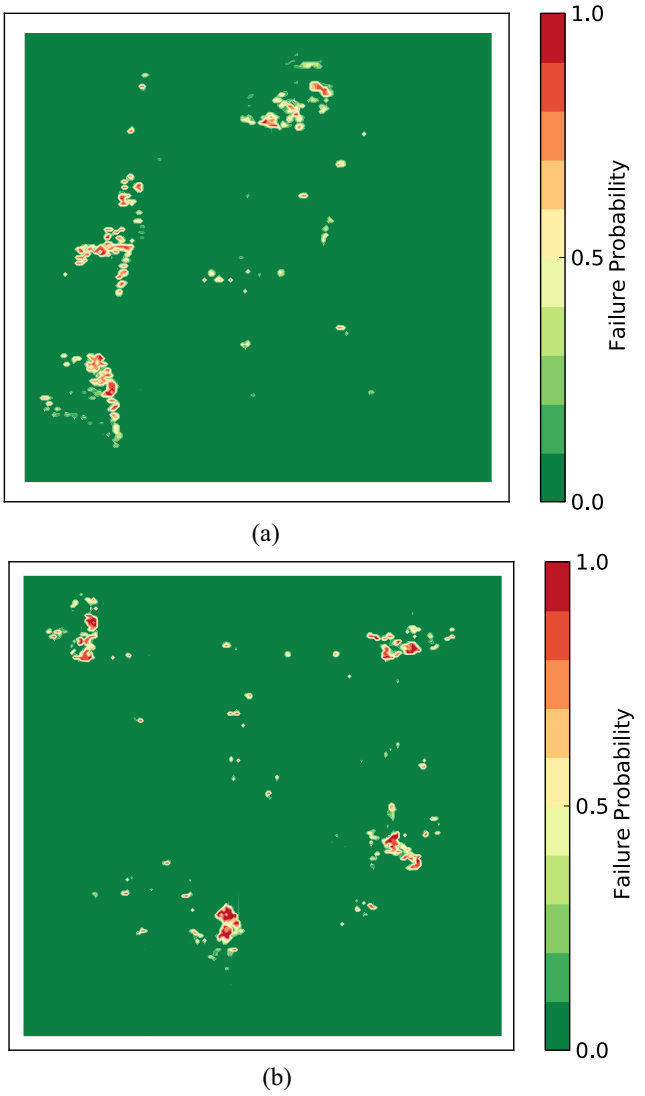

Fig. 10. Heatmap of MT failure probability for the layout of two benchmark circuits for two different particle energies. (a) b18 benchmark circuit and 22 MeV. (b) b19 benchmark circuit and 144 MeV.

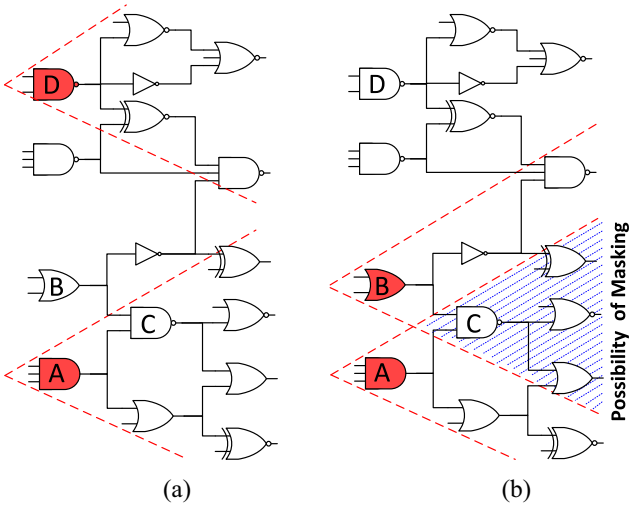

Fig. 11. Examples of errors with and without common gates in their forward cones. Errors with (a) nonoverlapped forward cones and (b) overlapped forward cones.

cells A and D have no common gates in their forward cones. Hence, the failure probability of MT affecting these two cells is $f_{AD} = 1-((1-f_A)(1-f_D))$. However, when there is an overlapped region in the forward cones of MT error sites, errors might interact with each other. In this case, it is possible that the effect of errors become less or more depending on the circuit structure and the running workload. For example, errors propagating from cells A and B may interact in cell C and the propagated errors to the output of this cell has significantly shorter pulse width than the errors generated at error sites. This phenomenon is known as pulse quenching and previous experiments showed that it is more probable specially for cells with GFI or GFO adjacency [34], [57]. Therefore, it is beneficial to identify netlist adjacent cells that could result in such error propagation behaviors and make them physically closer.

Based on the aforementioned optimization opportunities, we identify the pair of cells which could result in the MT masking and reduce their distance to mitigate MTs.

B. MT-Aware Placement Flow

In a typical place and route scenario, first an initial placement is obtained based on the netlist structure by exploiting a trial routing [56]. Although it is possible that the locations of some cells slightly change during the next phases (e.g., clock tree synthesis, timing optimization, and scan chain insertion) to resolve the congestion or timing violations, most of the cells remain in the same location. Thus, if MTs are mitigated in the initial placement, a similar effect is expected on the final layout as well.

The flow of our proposed MT-aware placement technique is depicted in Fig. 12. In this technique, the initial placement is first generated using a commercial place & route tool (e.g., Cadence SoC Encounter) by performing the trial routing. Then, local adjustments in the locations of the cells

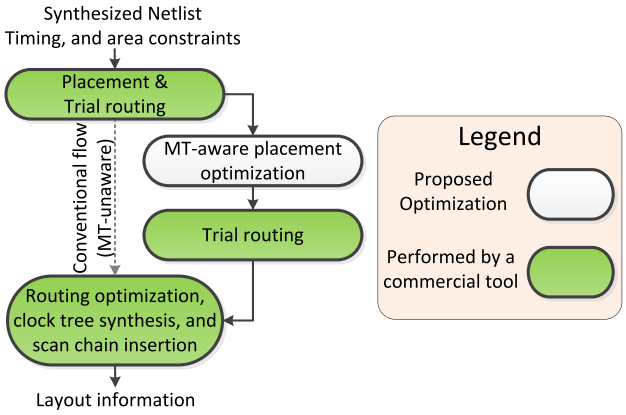

Fig. 12. Flow of the proposed MT-aware placement approach.

Algorithm 2: MT-Aware Placement Optimization

```
Read a layout from input
for each row in layout do
    for each adjacent cell pair i and j in row do
        f_i, f_j, and f_ij ← Compute joint and disjoint failure probabilities
        e_ij ← extract whitespace between cell i and j
        if f_ij < 1 − (1 − f_i)(1 − f_j) then
            white+ = e_ij
            e_ij ← 0
        else
            e_ij marked as ↑
        end
        Redistribute white among all e_ij s marked as ↑
        Change locations of cells in row
    end
end
Write a modified layout to a file
```

are performed to mitigate MTs, using the proposed algorithm. Afterwards, the modified placement is given back to the commercial tool to repeat the trail routing according to the modified cell locations. Then, the remaining layout generation steps are performed in the conventional way using a commercial tool. Using this approach, the final layout satisfies all the constraints and have smaller SER.

C. MT-Aware Placement Algorithm

In the conventional design flow, the standard cells have a constant size in at least 1-D that allows them to be lined up in rows on the layout. The layout consists of a large number of rows, each of which has a power and a ground line next to it and contains various cells as well as some whitespace. The proposed MT-aware placement technique accepts an existing placed design as an input and optimizes the location of cells within the row to reduce the average MT failure probability.

The proposed MT-aware placement technique neither moves the cells among different rows nor changes the order of cells in a row, rather it redistributes the existing whitespace in each row according to the vulnerability of the cells. The steps taken in the proposed MT-aware placement optimization technique are outlined in Algorithm 2. It analyzes the layout rows one by one. For each row, the adjacent cells in the row that could potentially result in error masking are first identified. In this regard, we compute the disjoint failure probability f_i, i.e., when only one cell is erroneous, for each cell i and joint failure probability f_{ij} considering when both adjacent cells i and j are

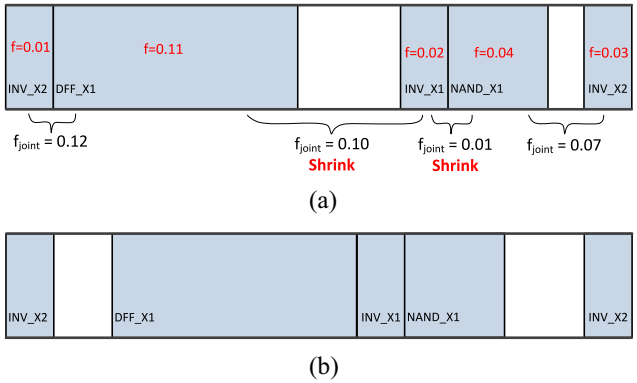

Fig. 13. Example of spacing before and after applying our MT mitigation technique. (a) Comparison of joint and disjoint vulnerabilities to decide on shrinkage/extension of empty space between cells. (b) Spacing after redistributing the spacing.

erroneous. For computing both joint and disjoint failure probabilities, the errors are propagated in the netlist according to the methodology described in Section III-B. In other words, the selection of the error sites for joint failure probability is based on the layout adjacency while error propagation is performed on the netlist-level.

According to Section V-A, if $f_{ij} < 1-(1-f_i)(1-f_j)$, there is a possibility of error masking when both cells are affected, hence, it is beneficial to remove the whitespace between the cells which satisfy this condition to increase the probability of such MT (lines 6–9). The eliminated whitespace have to be redistributed among the cell pairs which does not satisfy this condition as they introduce no masking. An example of whitespace redistribution is shown in Fig. 13. This whitespace redistribution reduces the probability of such MTs in the optimized layout. After analyzing all the rows in the layout and redistributing the whitespaces in the favor of MT mitigation, the modified layout structure is generated.

In this paper, we only adjust the locations of the cells within each row and we do not perform cell swapping across multiple rows. The main reason is to be compatible with the commercial tools. In this regard, the changes with respect to the original layout generated by the traditional placement flow must be both small and local, otherwise, the routing phase will have a considerable runtime and might not be able to find a solution for given area and timing constraints in a reasonable runtime.

VI. Experimental Results of MT-Aware Placement

In order to show the effectiveness of the proposed MT-aware placement technique, the layouts of several large circuits are optimized using this technique. In this section, the SER reduction, overheads, and runtime of this technique are presented. The process of preparations of the benchmark circuits and employed tools are similar to Section IV.

A. MT Mitigation

It is very important to notice that the ultimate objective of the MT-aware placement is to reduce the failure probability to be equal to the susceptibility to single transient errors (i.e., $f_{\text{SET/SEU}}$). In other words, the target is to reduce the gap between failure probability of MT with that of SET/SEU which is broadening with technology scaling. Hence, we introduce a metric called MT ratio reduction as follows:

$$\text{MT ratio reduction} = \frac{f_{\text{MT-unaware}} - f_{\text{MT-aware}}}{f_{\text{MT-unaware}} - f_{\text{SET/SEU}}} \quad (1)$$

where $f_{\text{MT-unaware}} - f_{\text{SET/SEU}}$ is the failure probability reduction potential (maximum achievable) and $f_{\text{MT-unaware}} - f_{\text{MT-aware}}$ is the actual reduction achieved by our technique. Based on this metric, 100% MT ratio reduction means that the SER of the system is equal to SET/SEU rate.

The failure probability of the optimized layout is computed using MC simulation similar to the original one, i.e., by placing the ovals in random locations, extracting the list of affected cells, and propagating errors. It worth to mention that the list of error sites is generated again for the optimized layout as the physical locations of the cells change during the optimization.

Fig. 14 shows the MT ratio reduction for the employed benchmark circuits synthesized for both Nangate 45 and 15 nm standard cell libraries. In this figure, the results for four particle energies (i.e., 22, 37, 95, and 144 MeV) are presented. As expected, by increasing the particle energy, the benefits of our proposed technique becomes less. However, since the particles with smaller energy are much more plentiful, the overall mitigation is mostly determined with respect to the reduction in particles with smaller energies. Also, it could be observed that the reduction ratio in 15 nm is slightly less than that of 45 nm. This could be explained by the average number of affected cells at these two technology nodes. As shown in Fig. 7(c), the average number of affected cells almost is doubled for all particle energies from 45 to 15 nm. Since the failure probability is computed with respect to all cells and our technique mitigates the errors for a subset of the cells, the failure probability reduction decreases by increasing the number of cells.

B. Overheads

The proposed technique only redistributes the existing whitespace in each row, hence, does not impose any area overhead. Additionally, it satisfies the given timing constraints similar to the MET-unaware placement. This is mainly because the locations of the cells are not fixed in MT-aware placement and could be changed when some of the constraints are not satisfied. During the experiments, the maximum operational frequency is obtained in MT-unaware approach for all benchmark circuits. Then, by putting the same timing constraints, the MT-aware placement is performed. The experimental results show no timing violations in the final layout.

C. Runtime

The proposed technique not only increases the runtime of the placement phase due to redistribution of the whitespaces, but also affect the runtime of the routing phase as trial routing has to be repeated after adjusting locations of the cells. The runtime of the place & route process for MT-unaware (conventional) and the proposed MT-aware placement are reported in Table IV. The MT-aware placement has 27.8%

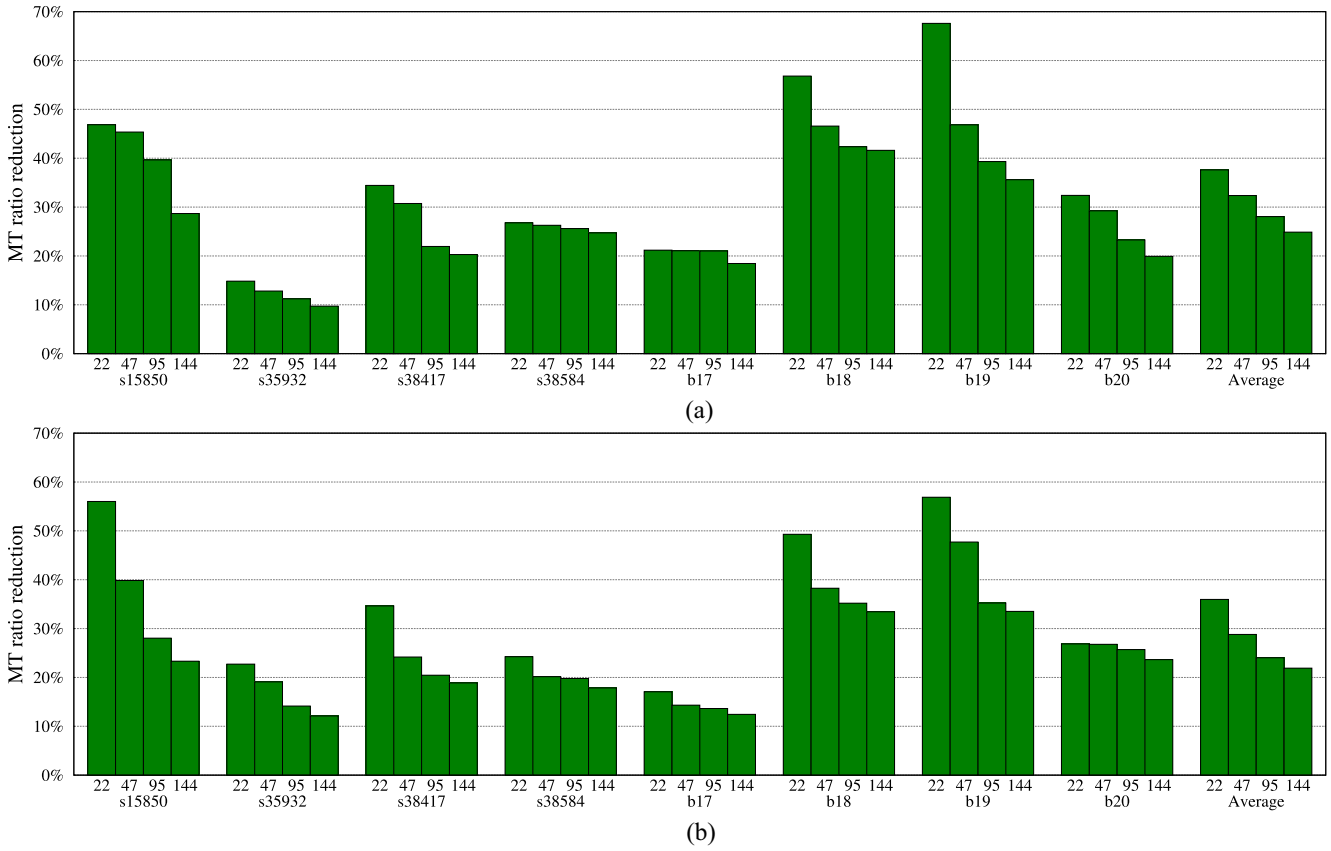

Fig. 14. MT failure probability reduction for benchmark circuits synthesized with respect to (a) 45 nm and (b) 15 nm Nangate standard cell library.

TABLE IV
COMPARISON OF RUNTIME MT-UNAWARE (CONVENTIONAL) AND MT-AWARE PLACE & ROUTE (P&R) [SECONDS]

Benchmark	MT-unaware P&R (SoC Encounter) Complete Execution	MT-aware P&R Initial P&R	MT-aware P&R Our Optimization	MT-aware P&R Final P&R	Runtime Overhead
s15850	189	102	3	134	26.5%
s35932	610	329	17	469	33.6%
s38417	614	297	23	362	11.1%
s38584	657	333	31	532	33.3%
b17	858	492	29	601	20.7%
b18	2,243	1,215	173	1,516	29.5%
b19	4,783	2,529	309	3,602	34.6%
b20	3,545	2,199	110	2,410	33.1%
Average					**27.8%**

longer runtime compared to the conventional approach, however, as it can be seen, this overhead is relatively constant for small and large circuits, hence, it is scalable to industrial-size circuits.

VII. CONCLUSION

In this paper, a fast and accurate layout-based SER estimation technique was presented. Unlike previous techniques in which the adjacent MT sites are obtained from logic-level netlist, we performed a comprehensive layout analysis to extract MT error sites. It is shown that the layout-based approach is the only viable solution for identification of adjacent cells as netlist-based techniques underestimate the overall SER of the circuit by up to 36.04%. We also presented an effective MT mitigation technique at the physical design step which optimizes the locations of the cells in the layout with respect to the MT vulnerability. Experimental results show that the proposed layout-based modeling and mitigation approaches have modest runtime and are scalable for industrial-size circuits.

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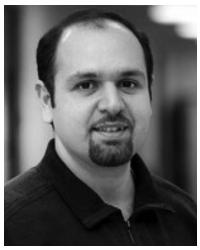

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